s nls

(FILE 'USPAT' ENTERED AT 06:28:19 ON 13 AUG 92)

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|---|---|---|---|
| L1 | 17355 | S | NON-VOLATILE OR NONVOLATILE |
| L2 | 24039 | S | REDUC?(P)STRESS |
| L3 | 9101 | S | LIMIT?(P)WRIT? |
| L4 | 208 | S | L1 AND L2 |
| L5 | 714 | S | L1 AND L3 |
| L6 | 11360 | S | REDUC?(5A)(STRESS OR WRIT?) |
| L7 | 4000 | S | LIMIT?(5A)(STRESS OR WRIT?) |
| L8 | 2526 | S | EEPROM OR ELECTRICALLY ERASABLE PROGRAMMABLE |
| L9 | 253 | S | L1 AND L6 |
| L10 | 162 | S | L1 AND L7 |
| L11 | 76 | S | L6 AND L8 |
| L12 | 91 | S | L7 AND L8 |
| L13 | 9417 | S | REDUC?(3A)(STRESS OR WRIT?) |
| L14 | 2778 | S | LIMIT?(3A)(STRESS OR WRIT?) |
| L15 | 51 | S | L8 AND L13 |
| L16 | 62 | S | L8 AND L14 |
| L17 | 7566 | S | REDUC?(2A)(STRESS OR WRITE) |
| L18 | 2023 | S | LIMIT?(2A)(STRESS OR WRIT?) |
| L19 | 5805 | S | REDUC?(1A)(STRESS OR WRIT?) |
| L20 | 46 | S | L8 AND L18 |
| L21 | 24 | S | L8 AND L19 |
| L22 | 0 | S | L20 AND CACH? |
| L23 | 0 | S | L21 AND CACH |
| L24 | 1 | S | L15 AND CACHE |
| L25 | 0 | S | L16 AND CACHE |
| L26 | 5 | S | L9 AND CACHE |
| L27 | 2 | S | L10 AND CACHE |
| L28 | 1 | S | L11 AND CACHE |
| L29 | 2 | S | L12 AND CACHE |

15

5,020,830

52

4933846

395/325

14

4713756

365/228

4,905,196

365/200

=> d l21 1-2 cit

1. 5,136,546, Aug. 4, 1992, Semiconductor memory; Minoru Fukuda, et al., 365/230.03, 189.05, 230.08 [IMAGE AVAILABLE]

2. 5,117,272, May 26, 1992, Having a protective film of a polymer having a fluorine-containing aliphatic cyclic structure; Shinzou Nomura, et al., 357/52, 54, 72 [IMAGE AVAILABLE]

=> d l28 cit

1. 4,905,196, Feb. 27, 1990, Method and storage device for saving the computer status during interrupt; Hubert Kirrmann, 365/200, 75

=> s l27 1-2 cit
MISSING OPERATOR 'L27 1-2'

=> d l27 1-2 cit

1. 5,051,887, Sep. 24, 1991, Maintaining duplex-paired storage devices during gap processing using of a dual copy function; Blaine H. Berger, et al., 395/425; 364/243, 246.6, 268, 268.1, 268.3, 268.5, 269.3, DIG.1 [IMAGE AVAILABLE]

2. 4,466,059, Aug. 14, 1984, Method and apparatus for limiting data occupancy in a **cache**; Arlon L. Bastian, et al., 395/250; 364/240, 240.2, 243, 243.4, 243.41, 243.43, 246, 246.1, 248.1, 261.3, 261.5, 263, DIG.1; 395/575 [IMAGE AVAILABLE]

d his

(FILE 'USPAT' ENTERED AT 11:05:30 ON 31 JUL 92)

L1 2228 S EEPROM OR ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY M
EMO

L2 [illegible]

L3 [illegible]

L4 266 S FLASH AND L1

L5 [illegible] L4 AND CACHE

L6 [illegible]

L7 31 S L1 AND CACHE

L8 368 S WRITE BACK BUFFER OR WRITE BUFFER

L9 5 S L7 AND L8

=> d l9 1-5 cit

1. 5,099,485, Mar. 24, 1992, Fault tolerant computer systems with fault isolation and repair; William F. Bruckert, et al., 371/68.3, 9.1 [IMAGE AVAILABLE]

2. 5,005,174, Apr. 2, 1991, Dual zone, fault tolerant computer system with error checking in I/O writes; William F. Bruckert, et al., 371/68.3; 364/228.3, 238.4, 240, 243.4, 243.41, 247, 259, 259.2, 263, 265, 265.5, 266.6, 268.3, 268.9, 269, 270, 270.5, 270.7, 271, 271.2, 280, 280.2, DIG.1; 395/575 [IMAGE AVAILABLE]

3. 4,953,930, Sep. 4, 1990, CPU socket supporting socket-to-socket optical communications; Bernard Ramsey, et al., 359/118; 357/40; 359/154; 385/147 [IMAGE AVAILABLE]

4. 4,916,704, Apr. 10, 1990, Interface of non-fault tolerant components to fault tolerant system; William F. Bruckert, et al., 371/68.3, 9.1 [IMAGE AVAILABLE]

5. 4,907,228, Mar. 6, 1990, Dual-rail processor with error checking at single rail interfaces; William F. Bruckert, et al., 371/68.3; 395/375, 575 [IMAGE AVAILABLE]

33. 4,794,521, Dec. 27, 1988, Digital computer with cache capable of concurrently handling multiple accesses from parallel processors; Michael L. Ziegler, et al., 364/200, 228.1, 228.2, 228.7, 228.9, 232.21, 243, 243.4, 243.41, 243.44, 243.6, 246, 246.3, 246.4, 247, 247.2, 247.3, 254, 254.3, 254.4, 256.3, 256.4, 258, 258.1, 258.2, 258.3, 258.4, 261.3, 261.6, 262, 262.1, 262.4, 262.8, 264, 264.1, 271.5, 280, 280.2, 281.3, 281.4, 281.7 [IMAGE AVAILABLE]

34. 4,783,736, Nov. 8, 1988, Digital computer with multisection cache ; Michael L. Ziegler, et al., 364/200, 228.3, 229, 229.2, 230, 230.1, 231.9, 234, 243, 243.4, 246, 246.4, 263 [IMAGE AVAILABLE]

35. 4,720,812, Jan. 19, 1988, High speed program store with bootstrap; Ming-Luh Kao, et al., 364/900, 925.6, 964.2, 965.76, 975.2 [IMAGE AVAILABLE]

36. 4,713,749, Dec. 15, 1987, Microprocessor with repeat instruction; Surendar S. Magar, et al., 364/200, 230.6, 237.81, 240, 240.2, 244.9, 259, 259.9 [IMAGE AVAILABLE]

37. 4,713,748, Dec. 15, 1987, Microprocessor with block move instruction; Surendar S. Magar, et al., 364/200 [IMAGE AVAILABLE]

38. 4,710,764, Dec. 1, 1987, Device for obtaining continuous plots on the screen of a display console controlled by a graphic processor; Luc P. Van Cang, 340/728, 721, 722, 747

39. 4,620,277, Oct. 28, 1986, Multimaster CPU system with early memory addressing; Jimmie L. Fisher, et al., 364/200, 228.3, 229, 229.2, 244, 244.6, 244.7, 245.5, 245.7, 251, 251.1, 251.3, 256.8, 259, 259.2, 264, 264.2 [IMAGE AVAILABLE]

40. 4,500,965, Feb. 19, 1985, Capstanless magnetic tape drive with electronic equivalent to length of tape; Martin D. Gray, 364/400; 360/55; 364/900, 932, 932.2, 932.4, 932.6, 939, 939.4, 947, 947.4, 948.3, 952, 952.4, 952.6, 959.1, 959.2, 964, 964.2, 965, 965.76, 968 [IMAGE AVAILABLE]

41. 4,498,155, Feb. 5, 1985, Semiconductor integrated circuit memory device with both serial and random access arrays; G. R. Mohan Rao, 365/230.09, 221, 240

42. 4,497,020, Jan. 29, 1985, Selective mapping system and method; Thomas J. Gilligan, 364/200, 238, 238.3, 243, 243.1, 244, 244.6, 246, 246.3, 252.3, 252.4, 259, 259.2, 265, 265.3, 266, 268, 268.3, 268.5 [IMAGE AVAILABLE]

43. 4,347,587, Aug. 31, 1982, Semiconductor integrated circuit memory device with both serial and random access arrays; G. R. Mohan Rao, 365/230.09, 215, 221, 240

44. 4,330,852, May 18, 1982, Semiconductor read/write memory array having serial access; Donald J. Redwine, et al., 365/221, 205, 240

45. 4,322,635, Mar. 30, 1982, High speed serial shift register for MOS integrated circuit; Donald J. Redwine, 377/54; 365/189.12, 240

46. 4,321,695, Mar. 23, 1982, High speed serial access semiconductor memory with fault tolerant feature; Donald J. Redwine, et al., 365/174, 185, 200, 240

47. 4,310,885, Jan. 12, 1982, Point of sale terminal having prompting display and automatic money handling; Noris S. Azcua, et al., 364/405, 900, 917.5, 917.7, 918, 918.5, 927.2, 927.4, 927.7, 927.8, 927.83, 928, 928.1, 928.2, 930, 932, 932.8, 943.1, 948.1, 948.2, 948.22, 949, 959.1,

d 12 1-50 cit

1. 5,051,887, Sep. 24, 1991, Maintaining duplex-paired storage devices during gap processing using of a dual copy function; Blaine H. Berger, et al., 364/200, 243, 246.6, 268, 268.1, 268.3, 268.5, 269.3 [IMAGE AVAILABLE]

2. 5,023,934, Jun. 11, 1991, Apparatus and method for communication of visual graphic data with radio subcarrier frequencies; Jesse Wheeless, 455/45, 23, 54, 72 [IMAGE AVAILABLE]

3. 5,023,847, Jun. 11, 1991, Boom event analyzer recorder; Robert A. Lee, 367/136; 235/400; 367/906 [IMAGE AVAILABLE]

4. 5,023,828, Jun. 11, 1991, Microinstruction addressing in high-speed CPU; William J. Grundmann, et al., 364/900, 231.8, 243.42, 244.3, 247.7, 254.5, 933.6, 939.7, 948.31, 957.6, 965.4 [IMAGE AVAILABLE]

5. 5,019,967, May 28, 1991, Pipeline bubble compression in a computer system; William R. Wheeler, et al., 364/200, 231.8, 262.4, 263, 271.5 [IMAGE AVAILABLE]

6. 5,014,235, May 7, 1991, Convolution memory; Steven G. Morton, 364/900, 754, 923.5, 927.8, 939.3 [IMAGE AVAILABLE]

7. 5,010,522, Apr. 23, 1991, Integrated-circuit configuration having fast local access time; Benjamin H. Ashmore, Jr., 365/189.07, 189.05 [IMAGE AVAILABLE]

8. 5,008,900, Apr. 16, 1991, Subscriber unit for wireless digital subscriber communication system; David N. Critchlow, et al., 375/8; 370/72; 375/11, 13 [IMAGE AVAILABLE]

9. 5,006,980, Apr. 9, 1991, Pipelined digital CPU with deadlock resolution; Douglas E. Sanders, et al., 364/200, 230, 231.8, 262.8 [IMAGE AVAILABLE]

10. 5,003,463, Mar. 26, 1991, Interface controller with first and second buffer storage area for receiving and transmitting data between I/O bus and high speed system bus; Richard W. Coyle, et al., 364/200, 228.5, 238, 238.3, 239, 239.4, 239.6, 239.7, 240, 240.3, 251.3, 270.2 [IMAGE AVAILABLE]

11. 4,996,697, Feb. 26, 1991, Deglitching means for digital communication systems; David N. Critchlow, et al., 375/104; 455/223 [IMAGE AVAILABLE]

12. 4,994,802, Feb. 19, 1991, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 341/122, 155 [IMAGE AVAILABLE]

13. 4,971,434, Nov. 20, 1990, Method for diagnosing deficiencies in and expanding a person's useful field of view; Karlene K. Ball, 351/224, 226 [IMAGE AVAILABLE]

14. 4,970,640, Nov. 13, 1990, Device initiated partial system quiescing; Brent C. Beardsley, et al., 364/200; 371/11.3 [IMAGE AVAILABLE]

15. 4,959,860, Sep. 25, 1990, Power-on password functions for computer system; Jeffrey S. Watters, et al., 380/4, 25 [IMAGE AVAILABLE]

measures the amplitude of each alignment signal. The amplitudes are used to determine analog and digital filter correction coefficients. Thereafter, input signals on the signal channel are filtered such that the combined amplitude response of the signal channel and filter is substantially flat over a designated frequency range.

4. 4,876,647, Oct. 24, 1989, Apparatus for determining water stress in crops; Bronson Gardner, et al., 364/420 [IMAGE AVAILABLE]

US PAT NO: 4,876,647 [IMAGE AVAILABLE] L3: 4 of 8

ABSTRACT:
An apparatus for determining the water stress condition of an agricultural crop growing in a field includes sensors for sensing environmental and crop conditions, such as air temperature, crop canopy temperature and relative humidity, and for generating signals indicative of the sensed conditions, a microprocessor for receiving the generated signals and for calculating a crop water stress index from the signals and a visual display for displaying, in the field, the calculated index. In one embodiment, the sensors are mounted in a pistollike, hand held housing and the microprocessor, display and a keyboard control are carried by a second housing. The microprocessor compares one or more of the sensed conditions to reasonable value limits and rejects a set of measurements containing values beyond the limits. Crop-specific data needed to calculate water stress indices for a particular crop are stored in a programmable, read only memory. When data for a different crop are needed, the memory may be removed and replaced by a memory containing the appropriate crop data, or, if erasable, the memory may be erased and reprogrammed for the different crop. The apparatus preferably includes a memory for storing a number of calculated crop water stress indices, each calculated from conditions sensed on a different day, in records including the date of the measurements. The stored indices can be retrieved and displayed with their measurement dates so that historical trends of crop water stress may be discerned.

5. 4,860,254, Aug. 22, 1989, Non-volatile electronic memory; Richard Pott, et al., 365/145; 357/40, 41; 365/129, 182 [IMAGE AVAILABLE]

US PAT NO: 4,860,254 [IMAGE AVAILABLE] L3: 5 of 8

ABSTRACT:
A volatile semiconductor memory module (RAM) is combined with a permanent memory based on an electrically polarizable, preferably ferroelectric, layer within an integrated monolithic module in such a manner that, as a result of a STORE command, the information present in the semiconductor memory is permanently stored by polarization of selected regions of the electrically polarizable layer. In the same way the permanently stored information can be read out again as a result of a RECALL command and returned to the semiconductor memory. Preferably, a ferroelectrically polarizable layer 11 is applied to the semiconductor memory, which layer, in the same way as the semiconductor memory, is provided on its upper side and underside with word and bit lines in the form of strip electrodes, 9,12. The strip electrode system 9 on the underside of the ferroelectric layer 11 simultaneously forms the word or bit line system of the semiconductor memory facing the surface. In this manner each semiconductor memory cell 7 is clearly allocated a non-volatile ferroelectric memory cell 13.

6. 4,829,296, May 9, 1989, Electronic lock system; Carey S. Clark, et al., 340/825.31; 70/77; 232/7; 235/382; 340/825.34 [IMAGE AVAILABLE]

US PAT NO: 4,829,296 [IMAGE AVAILABLE] L3: 6 of 8

ABSTRACT:
An electronic lock system adapted for use with receivers, such as parking meters, that include storage means and an electronically operable

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     (FILE 'USPAT' ENTERED AT 14:35:44 ON 21 OCT 91)
L1          148 S 364/273.4/CCLS
L2          129 S 364/268.9/CCLS
L3          147 S 364/948.5/CCLS
L4           48 S 364/945.3/CCLS
L5           59 S 364/944.61/CCLS
L6           16 S L1 AND L2
L7            4 S L1 AND EEPROM
L8            6 S L2 AND EEPROM
L9           11 S L3 AND L5
L10           9 S L3 AND EEPROM
L11           1 S L4 AND EEPROM
L12           2 S L5 AND EEPROM
L13           1 S 5043940/PN
                SEL L13 UREF 1
                EDIT E11-E17 "UREF" "PN"
                EDIT E11-E17 "," ""
L14           7 S E11-E17

=>
Session canceled by user request.
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d his

     (FILE 'USPAT' ENTERED AT 14:35:44 ON 21 OCT 91)
L1           148 S 364/273.4/CCLS
L2           129 S 364/268.9/CCLS
L3           147 S 364/948.5/CCLS
L4            48 S 364/945.3/CCLS
L5            59 S 364/944.61/CCLS
L6            16 S L1 AND L2
L7             4 S L1 AND EEPROM
L8             6 S L2 AND EEPROM
L9            11 S L3 AND L5
L10            9 S L3 AND EEPROM
L11            1 S L4 AND EEPROM
L12            2 S L5 AND EEPROM

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=> d 126 1-5 cit

1. 5,124,987, Jun. 23, 1992, Logical track write scheduling system for a parallel disk drive array data storage subsystem; Charles A. Milligan, et al., 371/10.1 [IMAGE AVAILABLE]

2. 5,119,485, Jun. 2, 1992, Method for data bus snooping in a data processing system by selective concurrent read and invalidate **cache** operation; William B. Ledbetter, Jr., et al., 395/425; 364/DIG.1 [IMAGE AVAILABLE]

3. 4,916,605, Apr. 10, 1990, Fast write operations; Brent C. Beardsley, et al., 395/425; 364/230.6, 238.2, 239, 239.8, 241.9, 243, 243.4, 243.41, 246, 246.1, 246.11, 246.12, 246.13, 260, 260.3, 264, 264.6, 268, 268.2, 268.3, 285, 285.1, 285.2, 430; DIG.1 [IMAGE AVAILABLE]

4. 4,905,196, Feb. 27, 1990, Method and storage device for saving the computer status during interrupt; Hubert Kirrmann, 365/200, 75

5. 4,466,059, Aug. 14, 1984, Method and apparatus for limiting data occupancy in a **cache**; Arlon L. Bastian, et al., 395/250; 364/240, 240.2, 243, 243.4, 243.41, 243.43, 246, 246.1, 248.1, 261.3, 261.5, 263, DIG.1; 395/375 [IMAGE AVAILABLE]

=> s 123 cit
MISSING OPERATOR 'L23 CIT'

=> d 123 cit
'L23' HAS NO ANSWERS
L8 2326 SEA EEPROM OR ELECTRICALLY ERASABLE PROGRAMMABLE
L19 5805 SEA REDUC?(1A)(STRESS OR WRIT?)
L21 24 SEA L8 AND L19
L23 0 SEA L21 AND CACH

password

actuator for providing access to material such as coins contained within the storage means in response to an electronic actuation signal. The electronic lock system comprises an access device and an electronic lock associated with each receiver. The access device includes means for storing a plurality of access codes such that each access code is associated with a unique identification code. Each electronic lock comprises means for storing a particular identification code and a passcode, and identification code means for providing the particular identification code. The access device also includes access code means for receiving the particular identification code and for providing the associated particular access code. The electronic lock further includes code comparison means for receiving the particular access code and comparing the particular access code to the passcode and for providing the actuation signal if the two correspond.



7. 4,712,427, Dec. 15, 1987, Vibrating beam accelerometer with velocity change output; Rex B. Peters, 73/517AV

US PAT NO: 4,712,427 L3: 7 of 8

ABSTRACT:
A dual sensor, frequency output accelerometer that does not require either high sampling rates or mechanical matching of the sensors to achieve high levels of accuracy. In one embodiment, the accelerometer comprises a first sensor (12, 14, 16) that produces an output signal S.sub.1 having a frequency f.sub.1 related to acceleration along the sensitive axis, and a second sensor (18, 20, 22) that produces a second signal S.sub.2 having a frequency f.sub.2 related to acceleration along the sensitive axis, the sensors being arranged such that a given acceleration causes the frequency of one output signal to increase and the frequency of the other output signal to decrease. Velocity change .DELTA.V during time interval T is determined according to:

$$\Delta V = A[\Delta\Delta\phi + FT + B\Sigma\Delta\phi]$$

where A, F and B are constants, .DELTA..phi. is the difference between the phase changes of the output signals over time interval T, and .SIGMA..phi. is the sum of the phase changes of the output signals over time interval T. Higher order correction terms are also described for very high precision applications. Also disclosed is an accelerometer or measuring velocity change during a time interval that includes a subinterval during which electrical power is unavailable.

8. 4,684,245, Aug. 4, 1987, Electro-optical coupler for catheter oximeter; Stanley D. Goldring, 356/41; 128/634, 665; 364/413.09, 571.04; 385/76 [IMAGE AVAILABLE]

US PAT NO: 4,684,245 [IMAGE AVAILABLE] L3: 8 of 8

ABSTRACT:
An optical module couples a fiberoptic catheter to a catheter oximeter processing apparatus. The module includes a plurality of LED's for coupling the electrical control signals from the processor and converting them to light signals to transmit to the catheter. The module also includes the means to convert the received reflected light signals from the catheter to electrical signals to be transmitted to the processor. The module further includes a memory to store calibration signals and other data so that the module and catheter can be disconnected from the processor and used with a different processor without necessitating a recalibration.

48. 4,308,615, Dec. 29, 1981, Microprocessor based maintenance system; Robert J. Koegel, et al., 371/16.1; 364/900, 919, 919.4, 921.8, 927, 927.2, 927.5, 927.8, 927.82, 928, 928.2, 931, 931.4, 932.8, 934, 937, 939, 939.5, 940, 940.1, 940.2, 941, 941.2, 942.7, 943.9, 945.4, 945.5, 945.7, 948.2, 949, 959.1, 965, 965.5, 965.76; 371/29.1 [IMAGE AVAILABLE]

49. 4,281,401, Jul. 28, 1981, Semiconductor read/write memory array having high speed serial shift register access; Donald J. Redwine, et al., 365/189.12; 357/40; 365/221, 222

50. 4,249,552, Feb. 10, 1981, Automatic money handling device; George D. Margolin, et al., 194/207, 206; 271/272

=> d l3 1-8 cit,ab

1. 5,047,772, Sep. 10, 1991, Digital error correction system for subranging analog-to-digital converters; David B. Ribner, 341/156, 118, 120, 161 [IMAGE AVAILABLE]

US PAT NO: 5,047,772 [IMAGE AVAILABLE] L3: 1 of 8

ABSTRACT:
A general architecture to correct conversion errors of a multi-stage, pipelined subranging analog-to-digital (A/D) converter includes cascaded stages, each stage generating a binary conversion signal representing the nearest quantized level below that of the analog input signal and a residual analog signal applied to the next conversion stage. The binary conversion signal from each stage addresses individual or common look-up tables providing a compensated binary signal selected to compensate for nonidealities of the A/D converter components. The compensated binary signals from the look-up tables provide a corrected output signal when summed together. A simple method of calibration for the A/D converter makes use of a least-mean-squared adaptation algorithm. The A/D converter accommodates practical circuit nonidealities such as component mismatching, gain error and voltage offsets, and handles high levels of amplifier nonlinearity. The architecture is applicable to any subranging converter with arbitrary numbers of stages and bits per stage.

2. 4,947,928, Aug. 14, 1990, VAV system coordinator; Edward Parker, et al., 165/22; 236/49.3 [IMAGE AVAILABLE]

US PAT NO: 4,947,928 [IMAGE AVAILABLE] L3: 2 of 8

ABSTRACT:
A microcomputer-based system coordinator for variable air volume (VAV) system through which conditioned air is supplied to a plurality of zones. The VAV system coordinator (VSC) is used to coordinate a central system VAV cooling and heating operation based on the zone requirements of its associated slave thermostats and fan box monitors. The VSC is used as a slave VSC which receives information from zone thermostats and fan box monitors and communicates with a master VSC which is used for overall system coordination. The VSC also receives information from temperature and humidity sensors and the real time for use in system operation.

3. 4,899,365, Feb. 6, 1990, Apparatus and method for adaptive amplitude equalization; Robert G. Hove, 375/13; 333/18; 375/98

US PAT NO: 4,899,365 L3: 3 of 8

ABSTRACT:
Apparatus and method for amplitude equalization of a signal channel such as a telephone line that does not requir[redacted]djustments at the customer's premises. The equalization circuit receives a plurality of alignment signals at predetermined frequencies from the signal channel, and

16. 4,943,983, Jul. 24, 1990, Subscriber unit for wireless digital telephone system; David N. Critchlow, 375/84, 8, 56, 67 [IMAGE AVAILABLE]



17. 4,942,606, Jul. 17, 1990, Computer with improved keyboard password functions; Roger A. Kaiser, et al., 380/4; 340/825.31, 825.34; 380/25, 50 [IMAGE AVAILABLE]

18. 4,941,176, Jul. 10, 1990, Secure management of keys using control vectors; Stephen M. Matyas, et al., 380/21, 25, 45, 47 [IMAGE AVAILABLE]

19. 4,932,826, Jun. 12, 1990, Automated cartridge system; Michael E. Moy, et al., 414/277; 360/92; 414/281 [IMAGE AVAILABLE]

20. 4,928,245, May 22, 1990, Automated cartridge system; Michael E. Moy, et al., 364/513; 242/180; 360/71, 92; 364/478; 369/39 [IMAGE AVAILABLE]

21. 4,916,605, Apr. 10, 1990, Fast write operations; Brent C. Beardsley, et al., 364/200, 230.6, 238.2, 239, 239.8, 241.9, 243, 243.4, 243.41, 246, 246.1, 246.11, 246.12, 246.13, 260, 260.3, 264, 264.6, 268, 268.2, 268.3, 285, 285.1, 285.2, 430 [IMAGE AVAILABLE]

22. 4,893,317, Jan. 9, 1990, Digital signals and frequency correction in a digital wireless system; David N. Critchlow, et al., 375/97; 328/155; 375/120

23. 4,881,240, Nov. 14, 1989, AM equalizer circuit for digital systems; David N. Critchlow, et al., 375/15; 333/18; 375/13

24. 4,875,160, Oct. 17, 1989, Method for implementing synchronous pipeline exception recovery; John F. Brown, III, 364/200, 231.8, 242.1, 247.6, 256.3; 371/12 [IMAGE AVAILABLE]

25. 4,873,652, Oct. 10, 1989, Method of graphical manipulation in a potentially windowed display; John Pilat, et al., 364/518; 340/724, 750; 364/521

26. 4,868,734, Sep. 19, 1989, Variable rate improvement of disc cache subsystem; Thomas E. Idleman, et al., 364/200, 232.8, 236.2, 238.4, 243, 243.4, 243.41, 243.43, 248.1, 249 [IMAGE AVAILABLE]

27. 4,864,601, Sep. 5, 1989, Integrated voice data workstation; Wayne F. Berry, 379/96; 370/125; D14/144, 151, 241, 252

28. 4,864,511, Sep. 5, 1989, Automated cartridge system; Michael E. Moy, et al., 364/478; 242/180; 360/92; 369/39

29. 4,837,739, Jun. 6, 1989, Telemetry data processor; David C. McGill, et al., 364/900; 340/825.05; 364/925, 925.1, 925.6, 927.2, 927.92, 927.93, 929.2, 930, 931, 931.4, 931.44, 932.8, 935, 935.2, 935.4, 935.45, 935.46, 937.01, 940, 940.61, 940.62, 942, 942.04, 943.9, 945, 948.1, 948.3, 948.4, 948.5, 952, 952.1, 959.1, 964, 964.2, 964.34, 965, 965.4, 965.5, 965.76, 965.77, 966.1, 966.3, 968, 972, 976; 370/85.1, 94.1; 371/8.2 [IMAGE AVAILABLE]

30. 4,825,448, Apr. 25, 1989, Subscriber unit for wireless digital telephone system; David N. Critchlow, et al., 375/8; 332/103; 375/56, 67

31. 4,825,394, Apr. 25, 1989, Vision metrology system; Jerald K. Baamish, et al., 364/571.01; 356/147, 376; 364/525, 560

32. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.[illegible]67.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9, 269.2, 269.3, 280, [illegible].3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

value, the EEPROM goes into an erase mode. The EEPROM interprets a second address received from the microprocessor as indicating the location where data is to be stored in the EEPROM. The EEPROM generates an internal write pulse which remains active until the EEPROM receives a subsequent write instruction from the microprocessor. In this way, it is not necessary to generate a wait instruction to the microprocessor to halt the microprocessor while the EEPROM is storing data. Also, it is not necessary to provide additional circuitry to control whether the EEPROM goes into the erase or programming modes.

23. 4,964,080, Oct. 16, 1990, Three-dimensional memory cell with integral select transistor; Jyh-Cherng J. Tzeng, 365/185; 357/23.4, 23.5, 55 [IMAGE AVAILABLE]

US PAT NO: 4,964,080 [IMAGE AVAILABLE] L4: 23 of 36
DATE FILED: Mar. 9, 1990

ABSTRACT:
A three-dimensional floating gate memory cell including an integral select gate transistor is disclosed. Source and drain are formed in a silicon substrate wherein the drain is formed under a slot which has been etched into the body of the substrate. In this way, the channel defined between the source and drain has both horizontal and vertical regions. The cell also includes a floating gate, which is completely surrounded with insulation, and a control gate which is insulated above and extends over the floating gate. The control gate is also insulated above and extends over the vertical portion of the channel within the slot. This allows the second gate member to regulate the current flowing in the vertical portion of the channel; that is, the second gate member and the vertical channel section form an integral select device.

24. 4,958,317, Sep. 18, 1990, Nonvolatile semiconductor memory device and a writing method using electron tunneling; Yasushi Terada, et al., 365/104, 185, 189.04, 189.05 [IMAGE AVAILABLE]

US PAT NO: 4,958,317 [IMAGE AVAILABLE] L4: 24 of 36
DATE FILED: Jul. 27, 1988

ABSTRACT:
Externally inputted data of one word line is temporarily stored in a latch circuit. In the writing cycle, the data stored and held in the latch circuit is collectively written in memory transistors connected to the selected word line. On this occasion, 0 V is applied to one of the control gate and the drain of the memory transistor in which "0" is written and a high voltage V.sub.PP is applied to the other of the control gate and the drain. Therefore, not only in the erasing cycle but also in the writing cycle, the operation is carried out by the movement of charges caused by the electron tunneling.

25. 4,951,103, Aug. 21, 1990, Fast, trench isolated, planar flash EEPROMS with silicided bitlines; Agerico L. Esquivel, et al., 357/23.5, 23.14, 45, 59, 67 [IMAGE AVAILABLE]

US PAT NO: 4,951,103 [IMAGE AVAILABLE] L4: 25 of 36
DATE FILED: Jun. 3, 1988

ABSTRACT:
A non-volatie cross-point memory cell array comprises a trench isolated cross-point array of memory cells (10), which are electrically programmable and electrically FLASH eraseable, having diffused regions (28) operable as bitlines, each diffused region (28) traversed by a plurality of control gates (54) operable as wordlines. The diffused regions (28) undergo a silicidation pr[illegible]s to decrease their resistivity, and thereby increase the [illegible]d of the memory cell array. A tunnel oxide (18) is provided for electrical erasing and programming.

d 16 1-16 cit,ab

1. 5,021,950, Jun. 4, 1991, Multiprocessor system with standby function; Akihito Nishikawa, 364/200, 229.2, 242.92, 268.9 , 273.1, 273.4 [IMAGE AVAILABLE]

US PAT NO: 5,021,950 [IMAGE AVAILABLE] L6: 1 of 16

ABSTRACT:
A multiprocessor system is comprised of a bus and a plurality of processor modules. Each processor module includes a bus arbitration block, a bus access control block, an address output block, a data input/output block, a clock signal generating block, a stop request block for requesting the stop of supplying a clock signal, an operation processing block for processing data, and a stop control block. The stop control block stores the contents of the bus access (a type of the bus, the address and data concerning the access, etc.) as is made by the operation processing block when the clock signal is stopped, and to what clock of that access cycle the bus access proceeds. The stop control block controls the bus arbitration block to electrically disconnect the processor module from the bus. After the restart of supplying the clock signal, the bus arbitration block, the bus access control block, the address output block and the data input/output block are restored on the basis of the contents of the bus access. Then the bus access that was stopped is resumed from its beginning. When the number of clocks of the clock signal is equal to that stored in the memory block after the restart of supplying the clock signal, the stop control block supplies again the clock signal to the operation processing block. Subsequently, the operation processing block continues the bus access.

2. 4,819,149, Apr. 4, 1989, Distributed control system; Paul S. Sanik, et al., 364/132, 200, 221, 221.9, 222.1, 228.3, 228.5, 229, 229.2, 229.4, 229.41, 230, 230.4, 232.7, 232.8, 234, 234.4, 235, 236.2, 237.2, 237.3, 237.4, 237.8, 238, 238.4, 238.5, 239.9, 240, 240.1, 240.2, 240.8, 241, 241.1, 242.3, 242.5, 243, 243.3, 244, 244.6, 246, 246.3, 248.5, 260, 260.1, 265, 265.1, 268, 268.9 , 273.4 , 280, 280.2, 280.3, 284, 285, 285.3, 285.4 [IMAGE AVAILABLE]

US PAT NO: 4,819,149 [IMAGE AVAILABLE] L6: 2 of 16

ABSTRACT:
A hierarchical distributive control system is disclosed. The lowest level of the system is a stand alone controller with hot plug in capability, which can accept either analog or digital signals, scale these signal with input subroutines, perform any one of a number of algorithms to produce control signals or can manually produce control signals and output these control signals as either analog or digital signals to field devices. A plurality of controllers communicates with an associated condenser over duel parallel digital communication buses with a full echo, verify communication routine. The condenser contains all records for all controllers under its supervision and can download control information into any replaced controller. A subhost is interconnected to

then signaling transmission commencement.



6. 4,799,140, Jan. 17, 1989, Majority vote sequencer; Ronald P. Dietz, et al., 364/140, 136, 141, 200, 221, 222.4, 223, 223.1, 232.7, 232.8, 242, 243, 243.3, 244, 244.6, 259, 259.1, 260.4, 260.8, 262.4, 267, 267.9, 268, 268.3, 268.8, 268.9 , 269, 269.1, 270, 273, 273.4 , 280, 280.2; 371/36 [IMAGE AVAILABLE]

US PAT NO: 4,799,140 [IMAGE AVAILABLE] L6: 6 of 16

ABSTRACT:
An electronic sequencing system comprised of two groups of three identically operating sequencers and circuitry that combines the outputs of these sequencers so that accurate, flexible and reliable sequencing of devices is obtained. Each sequencer is comprised of a microprocessor, memory, and peripheral circuits. The individual sequencer outputs are combined such that at least one of the corresponding system outputs will activate the device to be sequenced if at least two of three corresponding individual sequencer outputs signal that the device should be activated. Additional reliability is obtained by combining the outputs of each group of the identically operating sequencers to control the devices to be sequenced. Reset circuitry is also provided to simultaneously reset the sequencers and to prevent premature outputs from activating the devices to be sequenced.

7. 4,695,946, Sep. 22, 1987, Maintenance subsystem for computer network including power control and remote diagnostic center; David A. Andreasen, et al., 364/200, 228.5, 229, 229.1, 240.8, 241, 241.2, 241.4, 241.9, 242.94, 244, 244.8, 259, 259.7, 265, 266, 266.3, 267, 267.4, 267.5, 267.7, 268, 268.9 , 269.2, 270, 270.3, 273, 273.4 , 280, 280.2, 281.9, 284, 284.4, 286, 286.1 [IMAGE AVAILABLE]

US PAT NO: 4,695,946 [IMAGE AVAILABLE] L6: 7 of 16

ABSTRACT:
A maintenance processor forms part of a computer network wherein the processor (also designated as the User Interface Processor) operates to initialize and maintain and communicate to remote diagnostic terminals for purposes of confirming integrity of the system and also for displaying data for locating any faults or problems in the network. The maintenance subsystem initiates start-up and self-test routines in a sequenced order for establishing the integrity of the units in the network. The subsystem includes means for testing two types of subsystems, that is, one having I/O controllers with self-test capability and another subsystem having I/O controllers without self-test capability. The UIP provides means for complete control of the network. It can interface the network to a remote service center where all operations such as power-up and initialization can be also effectuated.

8. 4,631,661, Dec. 23, 1986, Fail-safe data processing system; Wolfgang Eibach, et al., 364/200, 221.9, 229, 229.4, 230, 232.8, 237.2, 237.4, 238.1, 238.5, 239, 239.2, 260, 260.1, 260.3, 263, 265, 265.6, 266.5, 267, 267.1, 267.4, 267.5, 267.7, 268, 268.3, 268.4, 268.5, 268.7, 268.9 , 270.1, 271, 271.2, 273.4 , 280, 281.9; 902/38 [IMAGE AVAILABLE]

US PAT NO: 4,631,661 [IMAGE AVAILABLE] L6: 8 of 16

ABSTRACT:
A fail-safe multiprocessor system comprises processors connected through a switching unit which forms a data transfer channel between the processors. This switching unit comprises mechanical switches that can selectively connect peripheral units (e.g., display units) with one of the processors. The transfer device constitutes, from the standpoint of each of the connected processors, a normal peripheral unit. The switches are set either manually or automatically under program control by each of

system is reconfigured such that the high priority tasks together with their associated peripheral units are transferred from the failed processor to a processor which is still intact.

9. 4,611,289, Sep. 9, 1986, Computer power management system; Anthony F. Coppola, 364/492, 200, 221, 221.7, 234, 234.2, 242, 242.1, 246.6, 246.9, 248.1, 248.2, 259, 259.3, 268.9 , 269.2, 273, 273.3, 273.4 , 281.3, 281.6, 281.9; 371/66 [IMAGE AVAILABLE]

US PAT NO: 4,611,289 [IMAGE AVAILABLE] L6: 9 of 16

ABSTRACT:
A power management system is disclosed for providing power to one or more computers having provisions for communication with an external data source. A source of backup power, including a bank of batteries, is provided which is provided to the power bus during a utility power interruption. A microprocessor monitors the utility line and the energy remaining in the batteries and provides data signals to the computer in response to utility power interruption and to predetermined battery energy levels. The data signals enable the computer to transfer data to non-volatile media to prevent data loss. In one embodiment, two way data links are provided between the computers and the microprocessor, which also controls power cutoff switches connected to each computer. Each computer may signal the microprocessor to cutoff backup power after data has been transferred to non-volatile media.

10. 4,597,084, Jun. 24, 1986, Computer memory apparatus; Ronald E. Dynneson, et al., 371/51.1; 364/200, 228.3, 232.7, 240.1, 241.2, 242.6, 242.7, 252, 260, 260.2, 265, 265.1, 266.3, 267, 267.3, 267.7, 268, 268.1, 268.3, 268.9 , 271, 273.4 [IMAGE AVAILABLE]

US PAT NO: 4,597,084 [IMAGE AVAILABLE] L6: 10 of 16

ABSTRACT:
A fault-tolerant computer system provides information transfers between the units of a computing module, including a processor unit and a memory unit and one or more peripheral control units, on a bus structure common to all the units. Information-handling parts of the system, both in the bus structure and in each unit, can have a duplicate partner. The units of a module check incoming and outgoing signals for errors, signal other module units of a detected error, and disable the unit from sending potentially erroneous information onto the bus structure. Error detectors check the operation of the bus structure and of each system unit to provide information transfers only on fault-free bus conductors and between fault-free units. The computer system can operate in this manner essentially without interruption in the event of faults by using only fault-free conductors and functional units.

11. 4,484,275, Nov. 20, 1984, Multiprocessor system; James A. Katzman, et al., 364/200, 228.3, 228.5, 228.7, 229.2, 230.6, 231.8, 232.7, 238, 238.3, 239, 239.1, 239.7, 240, 240.2, 241, 241.2, 241.6, 242.3, 246, 246.3, 254, 254.3, 265, 265.5, 266.6, 267, 267.7, 268, 268.3, 268.7, 268.9 , 270, 270.4, 273.4 , 285, 285.3 [IMAGE AVAILABLE]

US PAT NO: 4,484,275 [IMAGE AVAILABLE] L6: 11 of 16

ABSTRACT:
An input/output system for a processor of the kind in which a processor module has a central processing unit, a memory, an input/output channel, and a plurality of device controllers for controlling the transfer of data between the processor module and the peripheral devices includes a star poll connection in which each device controller is provided with a signalling means for signalling its ider[illegible] in response to a poll operation, independently of other simila[illegible] connected device controllers such that any number of device controllers can be failed or powered off

without affecting the polling of the other device controllers. The data lines in an input/output bus are used both to transmit data and to transmit signals to reduce the total number of lines needed to connect the device controllers to the channel in the star poll connection. The system is a fault tolerant system which includes an enable bit in the port of each device controller. The bit can be reset to prevent that device controller from transmitting spurious signals which could interfere with interrupt requests being transmitted to the channel by other device controllers so that a failed device controller can be effectively removed from the system. A rank line arrangement is utilized in the priority selection scheme so that an additional group of controllers can be added in a way which requires the use of only one more line in the input/output bus and still allows each device controller to respond independently to poll operations.

12. 4,458,307, Jul. 3, 1984, Data processor system including data-save controller for protection against loss of volatile memory information during power failure; James C. McAnlis, et al., 364/200, 232.3, 232.8, 232.9, 235, 237, 238.4, 240, 240.1, 241.9, 242.6, 242.7, 242.93, 243, 243.7, 244, 244.3, 244.6, 246, 246.2, 246.3, 249.8, 252.3, 252.6, 259, 259.9, 260, 260.1, 260.2, 262.4, 262.8, 263.1, 268.9 , 270, 270.4, 271.5, 273.4 , 280, 280.8, 282, 284, 284.2, 285, 285.1, 285.2, 285.3; 365/228; 371/66 [IMAGE AVAILABLE]

US PAT NO: 4,458,307 [IMAGE AVAILABLE] L6: 12 of 16

ABSTRACT:
A data processing system, having a volatile main memory prepares for power supply failure, at the first instance of power supply potential falling below a predetermined limit, by readying its current task for restart, data-saving by storing the contents of volatile, processor registers in the main memory, and completing any non-postponable tasks. If power deficiency lasts for longer than a predetermined period, the memory is maintained by a battery power source if and only if data-saving has been completed. Restoration of power during the predetermined period causes instant reversal and restart, but after the elapse of the predetermined period, causes reversal and restart if and only if a data save has been completed, otherwise causing reinitialization.

13. 4,420,807, Dec. 13, 1983, Selectively holding data in a buffer for defective backing store tracks; Arthur H. Nolta, et al., 364/200, 236.2, 238.2, 241.9, 242.3, 243, 243.4, 243.41, 246, 246.1, 246.11, 246.12, 262.4, 262.5, 268, 268.9 , 269.2, 273.4 , 280, 284, 284.3, 285, 285.1, 285.3; 365/200 [IMAGE AVAILABLE]

US PAT NO: 4,420,807 [IMAGE AVAILABLE] L6: 13 of 16

ABSTRACT:
Data associated with a defective area of a backing store and stored in an alternate area, such as defective and alternate tracks in a direct access storage device, is selectively stored in a high speed buffer front store based upon usage of such data. A first replacement control governs buffer operation for data from good areas of the backing store, and a second independent replacement control governs buffer operation for data from alternate storage areas. Limitations are imposed on the amount of data subject to the second replacement control.

14. 4,356,550, Oct. 26, 1982, Multiprocessor system; James A. Katzman, et al., 364/200, 225, 225.2, 226.3, 228.3, 228.5, 229, 229.2, 230, 230.1, 231.4, 231.5, 231.6, 231.7, 231.8, 234, 235, 236.2, 236.3, 236.4, 237, 238, 238.3, 239, 239.1, 239.6, 239.7, 240, 240.5, 240.8, 240.9, 241.1, 241.9, 242.3, 242.94, 242.96, 244, 244.3, 244.6, 246, 246.1, 246.3, 246.6, 246.7, 247, 248.1, 248.2, 254, 254.3, 256.3, 256.5, 259, 259.2, 259.7, 260, 260.1, 263.2, 265, 265.1, 266.3, 268, 268.3, 268.7, 268.8, 268.9 , 270, 271, 273.4 , 280, 281.1, 281.3, 285, 285.1, 285.3 [IMAGE AVAILABLE]

US PAT NO: 4,356,550 [IMAGE AVAILABLE] L6: 14 of 16



ABSTRACT:
A multiprocessor system, the kind in which two or more separate processor modules are interconnected for two power supplies, provides the entire power for the device controller in the event the other power supply fails. The distributed power supply system permits any processor module or device controller to be powered down so that on-line maintenance can be performed in a power-off condition while the rest of the multiprocessor system is on-line and functional.
The multiprocessor system includes a memory system in which the memory of each processor module is divided into four logical address areas--user data, system data, user code and system code. The memory system includes a map which translates logical addresses to physical addresses and which coacts with the multiprocessor system to bring pages from secondary memory into primary main memory as required to implement a virtual memory system. The map also provides a protection function. It provides inherent protection among users in a multiprogramming environment, isolates programs from data and protects system programs from the actions of user program. The map also provides a reference history information for each logical page as an aid to efficient memory management by the operating system.
The multiprocessor system includes in the memory of each processor module an error detection and correction system which detects all single bit and double bit errors and which corrects all single bit errors in semiconductor memory storage.

15. 4,228,496, Oct. 14, 1980, Multiprocessor system; James A. Katzman, et al., 364/200, 187, 225, 225.2, 226.3, 228.3, 228.5, 229, 229.2, 230, 230.1, 231.4, 231.6, 231.8, 232.7, 232.8, 234, 235, 236.2, 236.3, 236.4, 237, 238, 238.3, 239, 239.1, 239.6, 240, 240.2, 240.5, 240.8, 240.9, 241.1, 241.9, 242.3, 242.5, 243, 243.4, 244, 244.3, 244.6, 244.8, 245.5, 245.9, 246, 246.1, 246.3, 246.6, 246.9, 248.1, 248.2, 248.3, 249, 254, 254.3, 256.3, 256.4, 259, 259.2, 259.7, 260.4, 260.7, 265, 265.1, 265.3, 266.3, 268, 268.3, 268.7, 268.8, 268.9 , 270, 273.3, 273.4 , 280, 280.8, 281, 281.3, 281.6, 281.8, 284, 284.3; 371/11.3, 66 [IMAGE AVAILABLE]

US PAT NO: 4,228,496 [IMAGE AVAILABLE] L6: 15 of 16

ABSTRACT:
A multiprocessor system the kind in which two or more separate processor modules are interconnected for parallel processing includes two redundant interprocessor buses dedicated exclusively to interprocessor communication. Any processor module may send information to any other processor module by either bus. The buses are shared in use by the processor modules on a time-sharing basis. Use of each bus is controlled by a special bus controller.
The multiprocessor system includes an input/output system having multi-port device controllers and input/output buses connecting each device controller for access by the input/output channels of at least two different processor modules. Each device controller includes logic which insures that only one port is selected for access at a time.
The multiprocessor system includes a distributed power supply system which insures nonstop operation of the remainder of the multiprocessor system in the event of a failure of a power supply for a part of the system. The distributed power supply system includes a separate power supply for each processor module and two separate power supplies for each device controller. Either one of the two power supplies provides the entire power for the device controller in the event the other power supply fails. The distributed power supply system permits any processor module or device controller to be powered down so that on-line maintenance can be performed in a power-off condition while the rest of the multiprocessor system is on-line and functional.
The multiprocessor system includes a memory system in which the memory of

data, system data, user code and system code. The memory system includes a map which translates logical addresses [illegible] addresses and which coacts with the multiprocessor system to bring pages from secondary memory into primary main memory as required to implement a virtual memory system. The map also provides a protection function. It provides inherent protection among users in a multiprogramming environment, isolates programs from data and protects system programs from the actions of user programs. The map also provides a reference history information for each logical page as an aid to efficient memory management by the operating system.
The multiprocessor system includes in the memory of each processor module an error detection and correction system which detects all single bit and double bit errors and which corrects all single bit errors in semiconductor memory storage.

16. 4,208,715, Jun. 17, 1980, Dual data processing system; Mitsuo Kumahara, et al., 364/200, 228.3, 230, 234, 235, 236.2, 237.2, 237.3, 238, 238.2, 238.4, 240, 240.1, 243, 244, 244.6, 248.1, 252, 267, 267.5, 268, 268.9 , 273.4 , 280, 281, 281.3 [IMAGE AVAILABLE]

US PAT NO: 4,208,715 [IMAGE AVAILABLE] L6: 16 of 16

ABSTRACT:
A dual data processing system comprising a first data processing unit having a first control unit and a first logic switching circuit; a second control unit having a second logic switching circuit; a pair of switch circuits coupled to the first and second logic switching circuits, respectively; adapter buffers to be coupled selectively to the first and second control units according to the operation of the switch circuits; a first power source for supplying electric power to the first control unit and the adapter buffers coupled thereto; and a second power source for supplying electric power to the second control unit and the adapter buffers coupled thereto. The switch circuits are operated to connect the adapter buffers selectively to the first and second control units so that load balance is kept between the first and second control units.

=> d l7 1-4 cit,ab

1. 4,845,632, Jul. 4, 1989, Electonic postage meter system having arrangement for rapid storage of critical postage accounting data in plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 200, 225, 225.1, 226.8, 232.8, 243, 243.3, 244.6, 244.8, 246, 246.3, 246.4, 252, 252.6, 270, 270.1, 273.4 , 273.5, 900, 918, 918.52, 925.6, 964, 965, 965.76, 965.79 [IMAGE AVAILABLE]

US PAT NO: 4,845,632 [IMAGE AVAILABLE] L7: 1 of 4

ABSTRACT:
A system for the nonvolatile storage of data, such as a postage meter system, employs a microcomputer coupled to two nonvolatile memories. The first nonvolatile memory requires data be applied to the nonvolatile data terminals for more than a predetermined time for data to be written into said nonvolatile memory while the second nonvolatile memory is of a type wherein data applied to the second nonvolatile memory data terminals for less than the predetrermined time is sufficient for data to be written into the second nonvolatile memory. The microcomputer operates under control of a program store to apply data to the first nonvolatile memory data terminals for at least a predetermined time under particular operating conditions and under other operating conditions to applying data to the nonvolatile memory data terminals and during the predetermined time to the second nonvolatile memory terminals.

2. 4,839,802, Jun. 13, 1989, Adaptation of computer to communication operation; Daniel C. Wonak, et al., 364/200, 222.2, 222.3, 228.5, 231, 232.8, 232.9, 234, 235, 237.2, 237.3, 237.4, 237.8, 238, 238.3, 238.5,

1. 4,989,130, Jan. 29, 1991, System for determining and storing valid status information received from cross coupled unit; Junichi Moriyama, et al., 364/200, 264.1, 268.4, 268.9 ; 371/8.1 [IMAGE AVAILABLE]

US PAT NO: 4,989,130 [IMAGE AVAILABLE] L8: 1 of 6

ABSTRACT:
An initial status setting system in a multi-unit system constructed of a plurality of units wherein at least a set of status data is held in registers in at least two of the plurality of units, both units indicating whether or not the set of status data held in each of the registers is valid. The output of each of the registers is applied to the other of the registers, and each of the registers is controlled so that only a valid set of status data is input thereto.

2. 4,974,144, Nov. 27, 1990, Digital data processor with fault-tolerant peripheral interface; William L. Long, et al., 364/200, 240.2, 268, 268.3, 268.7, 268.9 ; 371/8.2 [IMAGE AVAILABLE]

US PAT NO: 4,974,144 [IMAGE AVAILABLE] L8: 2 of 6

ABSTRACT:
A fault-tolerant digital data processing system comprises a first input-output controller which communicates with at least one peripheral device over a peripheral device bus having first and second input/output buses, each carrying data, address, control, and timing signals from the input/output controller to the peripheral device. A device interface is coupled to the first and second input/output buses and to an associated peripheral device for transferring information between the buses and the associated peripheral device. In normal operation, the device interface applies duplicate information signals synchronously and simultaneously to the input/output buses for transfer to the input/output controller. The device interface also receives, in the absence of fault, duplicative information signal synchronously and simultaneously from the first and second input/output buses.

3. 4,939,643, Jul. 3, 1990, Fault tolerant digital data processor with improved bus protocol; William L. Long, et al., 364/200, 238.3, 240.2, 268.9 [IMAGE AVAILABLE]

US PAT NO: 4,939,643 [IMAGE AVAILABLE] L8: 3 of 6

ABSTRACT:
A fault-tolerant digital data processor includes a peripheral device controller for communicating with one or more peripheral devices over a peripheral device bus having first and second input/output buses, each carrying data, address, control, and timing information. Each peripheral device includes a device interface for transferring information signals between the associated peripheral device and the peripheral bus. The peripheral device controller includes a strobe element connected with the first and second input/output buses for transmitting thereon duplicative, synchronous and simultaneous strobe signals. These strobe signals define successive timing intervals for information transfers along the peripheral bus. Information transfers are normally effected by the transmission of duplicate information signals synchronously and simultaneously on the first and second input/output buses. A transfer cycle element includes a scanner cycle element to determine an operational state of at least one of the peripheral devices connected to the peripheral bus; a command cycle element for executing a command cycle for controlling operation of an attached peripheral device; a read cycle element for effecting the transfer of data signals from the peripheral device to the input/output controller; and a write cycle element for transferring data signals from the input/output controller an attached peripheral device.

273.4 , 286, 286.1, 286.2 [IMAGE AVAILABLE]



US PAT NO: 4,839,802 [IMAGE AVAILABLE] L7: 2 of 4

ABSTRACT:
A communication adapter for a personal computer or computer terminal is interposed between the computer process unit and its accessory units, such as a keyboard, a printer and a display monitor; the adapter includes a data memory for storing data and actuation signals from the keyboard, from the process unit, and from a communication port on the adapter, together with transmission logic circuits for transmitting data from the memory through the communication port, and accessory logic circuits for supplying data from the memory to the printer and to the monitor. The adapter further includes a microprocessor with a program memory, responsive to signals from the keyboard, that actuates the adapter between a computer mode of operation in which the computer process unit is effectively connected to the accessory units for operation of the computer as if the adapter were not present, and a communication mode in which the adapter and the accessory units function as a telecommunication transceiver independent of the computer process unit. In the computer mode the adapter remains active as an automated telecommunication transceiver, recording incoming data from its communication port in the data memory and transmitting previously recorded data from the memory.

3. 4,839,792, Jun. 13, 1989, Portable electronic apparatus with a device for determining data validity; Yasuo Iijima, 364/200; 235/380; 364/222.5, 225, 225.2, 231, 231.1, 231.2, 232.8, 237, 237.2, 237.3, 243, 243.3, 245, 245.1, 246, 246.3, 254, 254.3, 260, 260.1, 260.4, 260.81, 265, 265.1, 266.3, 273.4 , 273.5 [IMAGE AVAILABLE]

US PAT NO: 4,839,792 [IMAGE AVAILABLE] L7: 3 of 4

ABSTRACT:
According to the portable electronic apparatus of the invention, when a data string is to be written in a data memory, information indicating whether the data string is valid or not is appended to the data string, and the data string is stored. When a read instruction is supplied from a portable electronic apparatus handling system, a CPU connected to the data memory appends the information, indicating validity or invalidity of the data string, to the start of the readout data string, and supplies the data string to the portable electronic apparatus handling system. When the data string supplied from the portable electronic apparatus handling system is to be written in the data memory, the CPU appends the information indicating invalidity to the data string and writes the data string, thereby updating the information indicating invalidity to information indicating validity after the completion of the data string writing.

4. 4,663,539, May 5, 1987, Local power switching control subsystem; Larry D. Sharp, et al., 307/38, 35, 64, 66; 361/90, 91; 364/200, 228.4, 228.5, 229, 232.9, 238.3, 273.1, 273.2, 273.3, 273.4 , 492, 493 [IMAGE AVAILABLE]

US PAT NO: 4,663,539 [IMAGE AVAILABLE] L7: 4 of 4

ABSTRACT:
Each digital module in a network is provided with a local power switching control subsystem wherein the local module uses a local power switching control logic card which controls main power and subordinate power units in a predetermined sequence. Power up/down conditions or incremental/decremental voltage conditions can be effected by a local operator or by an instruction from a remote master logic unit. The power subsystem can sense failure conditions and communicate this information to the remote master unit or to a local operator.

4. 4,819,159, Apr. 4, 1989, Distributed multiprocess transaction processing system and method; Dale L. Shipley, et al., 364/200, 230.6, 236.3, 238.4, 238.5, 239, 239.7, 242.4, 242.6, 242.92, 242.94, 242.95, 244, 244.8, 248.1, 265, 266.3, 267, 267.2, 267.4, 268, 268.3, 268.4, 268.5, 268.7, 268.9 , 269.2, 269.3, 280, 281.3, 281.8, 282.1, 282.4; 371/9.1 [IMAGE AVAILABLE]

US PAT NO: 4,819,159 [IMAGE AVAILABLE] L8: 4 of 6

ABSTRACT:
The method and means of fault-tolerant processing includes a plurality of system building blocks, each including a real-time processor and specialized processors and local non-volatile memory that are coupled to communicate internally within each of the system building blocks, which, in turn, communicate with one another over local-area network links, and communicate with the remainder of the system over an I/O bus controlled by an I/O processor. Transaction-based processing is under control of a transaction coordinator which permits all of the transaction operations to complete successfully and then alter stored data for the completed transaction, or not to alter any stored data if a transaction is not completed. The transaction coordinator maintains a record of the distributed file accesses required during processing of a transaction, and prevents other transactions from altering stored data during processing of a transaction.

5. 4,740,887, Apr. 26, 1988, Method and system for improving the operational reliability of electronic systems formed of subsystems which perform different functions; Mark Rutenberg, 364/184; 114/23; 364/186, 187, 200, 237.9, 238.3, 241.9, 244, 244.6, 265, 266, 268, 268.9 , 285, 285.3; 371/11.3, 36 [IMAGE AVAILABLE]

US PAT NO: 4,740,887 [IMAGE AVAILABLE] L8: 5 of 6

ABSTRACT:
A method and system for improving the reliability of an electronic system formed of subsystems which perform different functions. The electronic system is analyzed to determine which of the subsystems is most likely to cause a system failure and these subsystems are targeted for monitoring and/or correction by a microcontroller unit. The microcontroller unit monitors the inputs and outputs of the targeted subsystems and determines when an output is inappropriate for the corresponding input. When an error is detected, an error code is stored in memory for future reference. When the microcontroller is in a correcting mode, open collector drivers are used to make corrections for an error in a digital output. Where the error generated is for an analog output, a digital to analog converter circuit and voltage followers are employed to impress the correct analog signal on the inappropriate output. The method and system are particularly applicable to weapons systems due to the possibility of critical failures in those systems and the limited space available for using redundant circuitry to improve reliability. In particular, the method and system are applicable to the gyro control unit and the command control unit of a torpedo for monitoring and/or correcting for failures in those systems.

6. 4,635,195, Jan. 6, 1987, Power control network using reliable communications protocol; James H. Jeppesen, III, et al., 364/200, 221, 221.7, 229, 229.1, 229.3, 229.5, 230, 230.4, 238.4, 240.8, 241, 242.5, 265, 265.1, 265.6, 266.4, 266.6, 267, 267.6, 268, 268.9 , 273.2, 273.5, 284, 284.3; 370/92; 371/34 [IMAGE AVAILABLE]

US PAT NO: 4,635,195 [IMAGE AVAILABLE] L8: 6 of 6

ABSTRACT:
A power network control system has a plurality of digital modules interconnected. A master logic unit in the network communicates with a

reliable power control system for selectively (or generally) instructing modules to turn on or to turn off this ... power source.



=> d l9 1-11 cit,ab

1. 5,038,320, Aug. 6, 1991, Computer system with automatic initialization of pluggable option cards; Chester A. Heath, et al., 364/900, 929.2, 929.5, 944.61 , 945, 948.5 , 975.2, 976.4; 371/11.1

US PAT NO: 5,038,320 L9: 1 of 11

ABSTRACT:
A data processing system includes a planar board having a central processing unit (CPU), a main memory unit, and input/output (I/O) sockets or slots, each adapted to receive a selected one of a plurality of different and/or similar option cards. each card contains (or is connected to) and controls a respective peripheral device; and each card is pre-wired with an ID value corresponding to its card type. Software programmable option registers on each card store parameters such as designated default (or alternate) address information, priority levels, and other system resource parameters. A setup routine, during initial power-on, retrieves and stores the appropriate parameters in the I/O cards and also in slot positions in main memory, one position being assigned to each slot on the board. Each slot position is adapted to hold the parameters associated with the card inserted in its respective slot and the card ID value. That portion of main memory containing the slot positions is adapted to maintain the parameter and ID information by means of battery power when system power fails or is disconnected, i.e., a nonvolatile memory portion. Subsequent power-on routines are simplified by merely transferring parameters from the table to the card option registers if the status of all the slots has not changed since the last power-down, system reset, or channel reset.

2. 4,805,109, Feb. 14, 1989, Nonvolatile memory protection arrangement for electronic postage meter system having plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 466, 900, 918, 918.1, 918.52, 927.8, 939, 939.7, 941, 941.7, 942.7, 943.9, 943.91, 943.92, 944.61 , 948.3, 948.4, 948.5 , 964, 965, 965.5, 965.76, 966.1, 966.4, 975.2 [IMAGE AVAILABLE]

US PAT NO: 4,805,109 [IMAGE AVAILABLE] L9: 2 of 11

ABSTRACT:
A system for the nonvolatile storage of data, such as a postage meter system, includes a microcomputer coupled to an MNOS type nonvolatile memory and also coupled to an EEPROM type nonvolatile memory, each memory having address lines and data lines. The address lines and data lines of the two nonvolatile memories are coupled to microcomputer ports such that the MNOS memory data lines are always at a high value whenever the EEPROM memory is addressed for the purpose of either writing or reading. The EEPROM nonvolatile memory control terminals and the MNOS nonvolatile memory control terminals are coupled to different ports of the microcomputer. Access to the MNOS nonvolatile memory is achieved by input/output mapping techniques. Access to the EEPROM nonvolatile memory is achieved by memory mapping techniques. In this way, protection is provided against inadvertently accessing the wrong memory or wrong address while executing read/write instructions to a selected memory.

3. 4,654,821, Mar. 31, 1987, Automatic restart apparatus for a processing system; Theodore R. Lapp, 364/900, 917.5, 921, 921.3, 921.8, 925.6, 926.9, 928, 928.4, 928.5, 943.9, 944.6, 944.61 , 944.91, 945, 945.1, 945.2, 948.4, 948.5 , 948.91, 949, 949.2, 949.3, 950, 950.5, 964, 964.6, 965, 965.5, 965.76, 975.1, 975.2, 976, 976.4; 371/12, 62 [IMAGE AVAILABLE]

ABSTRACT:
An automatic loading apparatus for a processing system for restarting an application program upon sensing a software failure. The application program periodically executes at least one portion of a reset code which addresses a peripheral device controller. The peripheral device controller times the frequency of the access by the processing system to determine whether the application program is executing successfully. If the application program does not access the peripheral control device within the normal period of execution for the reset code then this is an indication of a failure of the software to execute in the right sequence or a halt to the processing of the application program. Upon a failure indication, the peripheral control device disconnects power to the processing system and then reconnects power to enable an auto-boot to reload the application program and restart the software execution.

4. 4,648,066, Mar. 3, 1987, Memory module; Terry L. Pitt, 364/900, 926.9, 926.92, 927.83, 929.2, 943.9, 944.61 , 945.3, 946, 948.4, 948.5 , 948.91, 949, 957, 957.2, 969, 969.4, 974 [IMAGE AVAILABLE]

US PAT NO: 4,648,066 [IMAGE AVAILABLE] L9: 4 of 11

ABSTRACT:
A self-contained, portable memory module for transferring configuration data from one programmable panel controller to another. An internal replaceable lithium battery is provided for powering the memory integrated circuit chip when the module is not connected to a powered controller. The battery and module are interconnected by a three wire battery lead that can be plugged into the module in either direction. The module also has a hinged case with molded feet allowing the module to be stored upright on a flat surface to prevent damage to the internal lithium battery. The module further comprises a connector, recessed for protection from static electrical discharges, for interfacing the module to the controller, and a special battery connector which allows battery replacement without loss of the stored data.

5. 4,633,431, Dec. 30, 1986, Arrangement for coupling digital processing units; Albrecht Bar, 364/900, 927.92, 929, 929.1, 935, 935.2, 935.4, 935.43, 935.45, 935.46, 940, 940.1, 940.61, 940.62, 940.92, 943.9, 944, 944.1, 944.2, 944.3, 944.6, 944.61 , 945.4, 948.1, 948.4, 948.5 , 950, 950.3 [IMAGE AVAILABLE]

US PAT NO: 4,633,431 [IMAGE AVAILABLE] L9: 5 of 11

ABSTRACT:
A data bus system in which digital processing modules are associated with the busses in matrix fashion is disclosed. The modules contain respective intelligent and autonomously operating coupling units, by which information distribution on the busses, fault detection and error processing may be transacted in a decentralized manner. The system is highly secure and fault-tolerant. A corresponding matrix bus system together with the corresponding current couplers can also connect power supplies associated with each of the modules to each other in the event of failure of the power supply in an individual module.

6. 4,584,663, Apr. 22, 1986, Apparatus for power-on data integrity check of inputted characters stored in volatile memory; Kowji Tanikawa, 364/900, 922, 927.2, 928, 933.62, 944.61 , 944.91, 947, 947.2, 948.4, 948.5 , 964, 965, 965.5, 965.76, 965.78; 365/201, 228; 371/10.1, 68.1 [IMAGE AVAILABLE]

US PAT NO: 4,584,663 [IMAGE AVAILABLE] L9: 6 of 11

ABSTRACT:
A memory data coincidence device includes a volatile read write memory

keyboard for supplying data to the read write memory. The device further includes a read only memory for storing [illegible] data capable of being stored in the read write memory and a central processor unit (CPU) which compares the data of the read write memory with all data of the read only memory before it reads data out of the read write memory. If no coincidence takes place, the CPU sends forth a signal denoting the condition that the read write memory is not backed up.



7. 4,578,774, Mar. 25, 1986, System for limiting access to non-volatile memory in electronic postage meters; Arno Muller, 364/900; 340/799, 814; 364/466, 918, 918.5, 918.52, 934.51, 934.61, 944.61 , 948.4, 948.5 , 949, 949.1, 949.96, 965, 965.76, 965.78, 965.8, 969, 969.4; 365/195; 371/62 [IMAGE AVAILABLE]

US PAT NO: 4,578,774 [IMAGE AVAILABLE] L9: 7 of 11

ABSTRACT:
A method and associated apparatus for limiting the erasing and writing of data in the non-volatile memory (NVM) of an electronic postage meter operated under microcomputer control to predetermined periods of time after the power up and during the power down cycles of the meter, comprising the steps and associated apparatus for providing an output power signal in response to the establishment of a power up voltage condition, generating an output pulse in response to the presence of the output power signal, presetting the width of the output pulse to provide sufficient time to erase the desired data words from the NVM, applying a bias enable signal to an NVM enable terminal during the duration of the output pulse, enabling the remaining terminals of the NVM during the duration of the output pulse to allow the erasure of data from the NVM, removing the output power signal in response to a power down voltage condition, interrupting the operation of the microcomputer in response to the removal of the output power signal to ready the microcomputer for writing data in NVM, applying the bias enable signal to the NVM enable terminal at the inception of the power down cycle, enabling the remaining terminals of the NVM to allow the writing of data into the NVM during power down for a predetermined time period, and biasing the terminals of the NVM during normal postage meter operation to preclude writing of data into and erasure of data from the NVM.

8. 4,484,307, Nov. 20, 1984, Electronic postage meter having improved security and fault tolerance features; Jesse T. Quatse, et al., 364/900, 918, 918.5, 918.52, 918.7, 918.9, 927.2, 927.83, 928, 928.1, 930, 931, 933, 933.7, 943.9, 944.2, 944.5, 944.6, 944.61 , 945.3, 945.4, 945.5, 947, 947.1, 947.4, 947.5, 948.4, 948.5 , 948.8, 948.91, 965, 965.1, 969, 969.2 [IMAGE AVAILABLE]

US PAT NO: 4,484,307 [IMAGE AVAILABLE] L9: 8 of 11

ABSTRACT:
A microcomputerized postage meter that provides high degrees of security and fault tolerance. The meter maintains data security under low power conditions by the use of functionally nonvolatile memory units. Register and other data which must survive normal and abnormal losses of power to the meter electronics are stored in dual redundant battery augmented memories (hereinafter designated BAMs). Upon detecting an error condition, the microcomputer writes an appropriate fault code to the BAMs. A mechanism for disabling the meter includes dual redundant flip-flops which are set to a "faulted" state upon detection by the microcomputer of a failure condition. These flip-flops are powered by the BAM batteries. They cannot be reset except by physical access to the meter interior, which access is only available to authorized personnel at the factory. The fault flip-flops are also set when the microcomputer fails to properly execute its own operating program. Once the meter has been set to a "faulted" state, the fault flip-flops hold two signals, MPCLR ans SYSCLR, true. The BAM contents may still be read out

of presently accessed data in the path responsive to a power failure signal. Portions of the memory are organized in a family of major, minor mode, data from two major loops being replicated into the direct path. The arrangement exhibits improved access times, improved data rates and is secure from power failure problems. Moreover, the memory organization permits the realization of large capacity chips without requiring block replication.

=> d l10 1-9 cit,ab

1. 4,977,537, Dec. 11, 1990, Dram nonvolatizer; Donald R. Dias, et al., 364/900, 948.5 , 964.9, 965.79, 968; 365/222, 228, 229 [IMAGE AVAILABLE]

US PAT NO: 4,977,537 [IMAGE AVAILABLE] L10: 1 of 9

ABSTRACT:
A nonvolatile memory subsystem includes DRAMs and a battery-backed controller chip. The controller chip monitors the system power supply level to ascertain power fault conditions. When a power fault is detected, the controller provides the DRAMs with both a regulated supply voltage and appropriately timed refresh signals.
After the system power supply has returned to specification, the controller continues to generate refresh control signals until the commands it to stop.

2. 4,805,109, Feb. 14, 1989, Nonvolatile memory protection arrangement for electronic postage meter system having plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 466, 900, 918, 918.1, 918.52, 927.8, 939, 939.7, 941, 941.7, 942.7, 943.9, 943.91, 943.92, 944.61, 948.3, 948.4, 948.5 , 964, 965, 965.5, 965.76, 966.1, 966.4, 975.2 [IMAGE AVAILABLE]

US PAT NO: 4,805,109 [IMAGE AVAILABLE] L10: 2 of 9

ABSTRACT:
A system for the nonvolatile storage of data, such as a postage meter system, includes a microcomputer coupled to an MNOS type nonvolatile memory and also coupled to an EEPROM type nonvolatile memory, each memory having address lines and data lines. The address lines and data lines of the two nonvolatile memories are coupled to microcomputer ports such that the MNOS memory data lines are always at a high value whenever the EEPROM memory is addressed for the purpose of either writing or reading.
The EEPROM nonvolatile memory control terminals and the MNOS nonvolatile memory control terminals are coupled to different ports of the microcomputer. Access to the MNOS nonvolatile memory is achieved by input/output mapping techniques. Access to the EEPROM nonvolatile memory is achieved by memory mapping techniques. In this way, protection is provided against inadvertently accessing the wrong memory or wrong address while executing read/write instructions to a selected memory.

3. 4,682,292, Jul. 21, 1987, Fault tolerant flight data recorder; Richard L. Bue, et al., 364/424.04; 360/5; 364/424.06, 900, 925, 925.1, 926, 933, 933.6, 943.9, 944.92, 947, 947.5, 948.4, 948.5 , 951.1, 951.3, 957, 957.7, 960, 960.7, 961, 965.79; 369/21; 371/2.1 [IMAGE AVAILABLE]

US PAT NO: 4,682,292 [IMAGE AVAILABLE] L10: 3 of 9

ABSTRACT:
Signal units of information stored in electronic memory are arranged in frames which are separated in memory by configurable end of data pointers, each frame stored with a first configuration pointer indicating a present frame, the storing of each present frame changing the preceding

BAMs. This is accomplished by allowing power necessary to read the BAMs to be supplied to the BAMs without supplying power to the microcomputer. Moreover, even if the microcomputer is powered, MPCLR prevents it from executing instructions and SYSCLR isolates it.



9. 4,275,456, Jun. 23, 1981, Betting tickets selling and collecting system; Takehiko Tanaka, et al., 364/900, 916.5, 920, 927.2, 928, 928.1, 930, 933, 933.7, 935, 935.2, 937, 937.1, 937.2, 940, 940.1, 942.7, 943.9, 944.61 , 945, 945.1, 945.3, 948.4, 948.5 , 962, 962.1, 967, 967.1 [IMAGE AVAILABLE]

US PAT NO: 4,275,456 [IMAGE AVAILABLE] L9: 9 of 11

ABSTRACT:
In a ticket selling and collecting system wherein a plurality of apparatus for selling betting tickets are connected in parallel to the data collecting apparatus, a memory which stores the latest ticket selling data which has been sent to the apparatus for selling betting tickets is provided in the data collecting apparatus. If a power failure occurs in the apparatus for selling betting tickets and thereafter power is restored the apparatus for selling betting tickets sends a message for requesting the latest ticket selling data to the data collecting apparatus and receives the latest ticket selling data from the memory of the data collecting apparatus, thereby the ticket selling information which has been invalidated by the power failure generated at the time of ticket selling can be reproduced accurately in the apparatus for selling betting tickets. Thus, the operator's burden due to power failure in the apparatus for selling betting tickets can be alleviated and an accurate collection file can be maintained.

10. 4,254,472, Mar. 3, 1981, Remote metering system; Richard O. Juengel, et al., 364/900; 340/870.03; 364/918, 918.1, 920, 921.8, 921.9, 923, 923.2, 926.9, 927.2, 927.5, 928, 928.1, 929, 929.2, 932.8, 934, 934.2, 935, 935.2, 935.4, 935.7, 936.1, 937.1, 937.2, 940, 940.1, 940.5, 942.1, 942.7, 942.8, 943.9, 944.61 , 944.8, 945, 945.1, 946.2, 946.6, 947, 947.2, 947.5, 948.1, 948.4, 948.5 , 948.91, 949, 949.1, 950, 950.1, 951.1, 951.4, 959.1, 964, 964.1, 965, 965.5, 965.8, 967, 967.1 [IMAGE AVAILABLE]

US PAT NO: 4,254,472 [IMAGE AVAILABLE] L9: 10 of 11

ABSTRACT:
A remote metering system for monitoring, collecting, analyzing, transmitting and displaying data generated by a plurality of metering devices. A controller, preferably a microprocessor, stores the continually up-dated data, analyzes it, and initiates transmission of the data to at least one remote data receiving device. The data transmission from the controller is in serial format and includes a plurality of different channels, with at least one channel corresponding to a combination of selected data associated with different metering devices. A scaling factor can be applied to particular metering data prior to transmission, for example, so as to provide cost analyses. The remote data receiving device includes the capability of receiving and displaying data corresponding to any of the output data transmission channels from the controller.

11. 4,237,544, Dec. 2, 1980, Magnetic memory organization; Peter I. Bonyhard, 364/900, 926.9, 942.7, 943.9, 944.61 , 945, 948.4, 948.5 , 951, 953, 953.1; 365/15, 74 [IMAGE AVAILABLE]

US PAT NO: 4,237,544 [IMAGE AVAILABLE] L9: 11 of 11

ABSTRACT:
A magnetic bubble memory herein includes a direct propagation path between a bubble generator and a detector. A control circuit is adapted

to it has a proper operating voltage level. Pulses produced in the message display system are counted to determine the sequential locations of data in the memory transfer unit to be transferred to the message display unit for substitution for data stored in the message display unit.

7. 4,564,922, Jan. 14, 1986, Postage meter with power-failure resistant memory; Arno Muller, 364/900, 917.5, 917.7, 918, 918.5, 918.52, 918.7, 927.2, 928, 935.2, 935.4, 935.45, 935.46, 940, 941, 948.4, 948.5 , 949, 959.1, 959.4, 964, 964.1, 965, 965.5, 965.76, 965.78 [IMAGE AVAILABLE]

US PAT NO: 4,564,922 [IMAGE AVAILABLE] L10: 7 of 9

ABSTRACT:
A security system for a postage meter includes two memories, one of which is an electronically programmable READ-ONLY memory having non-volatile storage, while the second memory is a shadow RAM which is a composite memory having a first section composed of a volatile RAM and a second section composed of non-volatile storage. During a power outage, a computer strobes the second memory to transfer data from the volatile section to the non-volatile section. Upon restoration of the power, a transfer circuit which includes a detector of the incoming power directs the transfer of at least a portion of the stored data in each of the memories to the computer for a comparison to determine if any data has been altered by the loss of power.

8. 4,523,295, Jun. 11, 1985, Power loss compensation for programmable memory control system; Thomas J. Zato, 364/900; 340/660, 661, 662, 663; 358/190, 335; 364/483, 925.6, 927.2, 927.4, 927.8, 934, 946.2, 946.6, 947, 947.6, 948.4, 948.5 , 949, 949.2, 952, 952.4, 952.5, 959.1, 964, 965, 965.5, 965.76 [IMAGE AVAILABLE]

US PAT NO: 4,523,295 [IMAGE AVAILABLE] L10: 8 of 9

ABSTRACT:
An arrangement for storing user programmed system timing information in a microprogrammable system in the event of a power outage. The system includes a static random access memory (RAM) for periodically storing microprocessor-generated timing information and an electrically erasable programmable ROM ( EEPROM ) which is coupled to the static RAM for the temporary storage of this information in the event of a power outage. Also provided in the system is a power down sensor responsive to an AC-coupled power supply for detecting power loss to the system. When the input voltage drops below a predetermined value, the contents of the static RAM are automatically transferred to the nonvolatile EEPROM . When system input power is restored, the stored contents of the nonvolatile EEPROM are automatically retransferred back to the static RAM for use by the microprocessor permitting the resumption of system operation as previously programmed on a time-shifted basis where the time shift equals the duration of the power outage. The system is particularly adapted for use with a user-programmed device, such as a television receiver or a video cassette recorder, in an environment where power outages of very short duration randomly occur. The present invention permits such a system to resume programmed system operation following resumption of power to the system without employing the combination of a battery, an oscillator, a CMOS RAM and appropriate recharging circuitry, as generally utilized in such systems.

9. 4,494,114, Jan. 15, 1985, Security arrangement for and method of rendering microprocessor-controlled electronic equipment inoperative after occurrence of disabling event; Norman Kaish, 340/825.31, 426, 571; 364/900, 918, 918.7, 919, 919.2, 920.5, 925, 925.2, 925.6, 927.2, 927.8, 928, 937, 948.4, 948.5 , 949, 949.96, 959.1, 964, 965, 965.5, 965.76, 969, 969.3, 969.4 [IMAGE AVAILABLE]

ABSTRACT:
A lock-out security arrangement for and method of maintaining microprocessor-controlled electronic equipment normally operational until the occurrence of a disabling event, such as physical removal of the equipment from its normal installation, and/or electrical removal of the equipment from a source of electrical power, and thereupon for disabling the equipment after detecting the disabling event and for maintaining the equipment disabled, even after the disabling event has been discontinued, until a code manually entered via a keyboard associated with a microprocessor for controlling the normal operation of the equipment matches a private access code whose identity is protected from external interrogation by reason of being stored in an internal non-volatile memory of the microprocessor. The private access code is preferably selected by and known only to the user, and may be changed to a different private access code at the user's option.

=> d l11 cit,ab

1. 4,791,603, Dec. 13, 1988, Dynamically reconfigurable array logic; Matthew R. Henry, 364/900; 307/465; 364/934, 934.4, 943.9, 945.3 , 948.1, 949.3, 949.4, 960, 960.2, 965, 965.77, 975.1 [IMAGE AVAILABLE]

US PAT NO: 4,791,603 [IMAGE AVAILABLE] L11: 1 of 1

ABSTRACT:
A dynamically reconfigurable array logic (DRAL) is capable of in-system logical reconfiguration in real time and comprises a RAM programmable logic array of bits, each bit comprising a fuse connection between logic elements. I/O means are coupled to the RAM programmable logic array for logical selection of registered output. A first register is coupled for receiving data and high-level commands. A sequencer includes a pair of up/down counters and functions to generate addresses. A timing device controls DMA transfers and issues READ and WRITE strobes. A second register monitors outputs and functions as a comparator, in a first mode, and functions to load outputs during specified time intervals in a second mode.

=> d l12 1-2 cit,ab

1. 4,817,004, Mar. 28, 1989, Electronic postage meter operating system; Paul C. Kroll, et al., 364/464.02, 900, 918, 918.1, 918.52, 939, 939.7, 943.9, 943.91, 944.2, 944.61 , 945.4, 945.7, 965, 965.76, 965.79, 976 [IMAGE AVAILABLE]

US PAT NO: 4,817,004 [IMAGE AVAILABLE] L12: 1 of 2

ABSTRACT:
A postage meter system includes a nonvolatile memory and program store coupled to a microcomputer. Postage meter transactional accounting data records are stored in the nonvolatile memory. Each transactional accounting data record includes a header portion having piece count related data and a piece count data field. The most current stored transactional accounting record header includes piece count related data which differs from the piece count data in the piece count field. Other stored transactional accounting records have headers with piece count related data which are the same as the piece count data stored in the piece count field. In this way, the most current record can be rapidly identified. A ring buffer organization of nonvolatile memory locations are utilized for storing postage value setting prior to the commencement of a postage dispensing transaction. By utilizing the ring buffer postage setting data and the most current postage transactional accounting record, a postage meter transaction can be reconstructed and written into a new postage transactional accounting record should a fault occur during a transaction which would preclude the writing of valid data. A program

2. 4,990,005, Feb. 5, 1991, Printer that prints a table of information about printing effects using the selected printing effects; Hiroyuki Karakawa, 400/76, 83, 703 [IMAGE AVAILABLE]

US PAT NO: 4,990,005 [IMAGE AVAILABLE] L2: 2 of 19

ABSTRACT:
A printer that can print a table of information about printing effects using the printing effects selected in an effects setting mode. For example, if the "emphasized" style is selected, a table with a fixed description of the printing effects is printed using the "emphasized" effect so that the printing effect can be confirmed visually. Further, if the printed effects deviate from the information in the table of printing effects, abnormalities of a memory or such are easily recognized.

3. 4,977,528, Dec. 11, 1990, Apparatus and method for determining the amount of material in a tank; Stephen G. Norris, 364/571.04; 73/1H, 3; 340/612, 618; 364/509 [IMAGE AVAILABLE]

US PAT NO: 4,977,528 [IMAGE AVAILABLE] L2: 3 of 19

ABSTRACT:
In order to determine the contents of a tank fitted with liquid level sensors and metering equipment, a microprocessor is programmed with an algorithm employing a mathematical expression for initially computing data value based on liquid level sensor outputs and tank dimensions, which data values are compared with actual volumetric amounts of liquid in the tank derived from the metering equipment so as to determine errors in a calibration characteristic for converting the sensor outputs into volumetric amounts. The calibration characteristic is refined by an iterative technique where constants in the mathematical expresson are varied, in accordance with the program so as to make the computed data values closer to the actual volumetric amounts derived from the metering equipment for respective liquid levels in the tank.

4. 4,951,763, Aug. 28, 1990, Checkweigher; Scott E. Zimmerman, et al., 177/164, 185 [IMAGE AVAILABLE]

US PAT NO: 4,951,763 [IMAGE AVAILABLE] L2: 4 of 19

ABSTRACT:
A method and apparatus for in-motion weighing is effectuated by a load cell combined with a means to filter the output thereof and apply the product to a programmable gain amplifier. The programmable gain amplifier's output is filtered and applied to a microprocessor which automatically regulates the programmable gain amplifier according to algorithms which results in an educable system responsive to basic operator initiation commands for determing and setting automatic in-motion weighing functions. Digital filter techniques are use to enhance overall system tolerances.

5. 4,947,454, Aug. 7, 1990, Radio with digitally controlled audio processor; Terry N. Garner, 455/84; 370/95.1; 455/88, 186, 249 [IMAGE AVAILABLE]

US PAT NO: 4,947,454 [IMAGE AVAILABLE] L2: 5 of 19

ABSTRACT:
A mobile radio is disclosed which includes an integrated circuit audio processor which operates under the control of at least one microprocessor. The audio processor provides basic transmit/receive audio filters, tone signaling filters, squelch filters, an RF power level control circuit, a DC voltage measuring circuit, a volume level adjusting circuit, and a transmit level adjusting circuit. In the audio processor, audio bandwidth, tone filter response, squelch filter response and other

accounting data into a random access memory, a second full set of critical accounting data and a set of abbreviated critical accounting data into the nonvolatile memory. The program store further causes the microcomputer, when an error is detected in at least one of the nonvolatile memory records, upon a comparison of data, where data in the random access memory is used as the accurate reference data, to rewrite data into both the full record and the abbreviated data record stored in the nonvolatile memory.

2. 4,805,109, Feb. 14, 1989, Nonvolatile memory protection arrangement for electronic postage meter system having plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 466, 900, 918, 918.1, 918.52, 927.8, 939, 939.7, 941, 941.7, 942.7, 943.9, 943.91, 943.92, 944.61 , 948.3, 948.4, 948.5, 964, 965, 965.5, 965.76, 966.1, 966.4, 975.2 [IMAGE AVAILABLE]

US PAT NO: 4,805,109 [IMAGE AVAILABLE] L12: 2 of 2

ABSTRACT:
A system for the nonvolatile storage of data, such as a postage meter system, includes a microcomputer coupled to an MNOS type nonvolatile memory and also coupled to an EEPROM type nonvolatile memory, each memory having address lines and data lines. The address lines and data lines of the two nonvolatile memories are coupled to microcomputer ports such that the MNOS memory data lines are always at a high value whenever the EEPROM memory is addressed for the purpose of either writing or reading.
The EEPROM nonvolatile memory control terminals and the MNOS nonvolatile memory control terminals are coupled to different ports of the microcomputer. Access to the MNOS nonvolatile memory is achieved by input/output mapping techniques. Access to the EEPROM nonvolatile memory is achieved by memory mapping techniques. In this way, protection is provided against inadvertently accessing the wrong memory or wrong address while executing read/write instructions to a selected memory.

to power interruption during storage is limited to the identifiable present frame.



4. 4,644,494, Feb. 17, 1987, Solid state memory for aircraft flight data recorder systems; Hans R. Muller, 364/900, 920, 922.5, 925, 925.1, 926, 927.2, 927.5, 932.8, 943.9, 944.92, 948.2, 948.3, 948.31, 948.4, 948.5 , 949.5, 953, 954, 957, 957.1, 960, 960.3, 960.6, 965, 965.76, 967, 967.3, 969, 969.2, 969.3, 970, 970.1, 977.5 [IMAGE AVAILABLE]

US PAT NO: 4,644,494 [IMAGE AVAILABLE] L10: 4 of 9

ABSTRACT:
A memory unit for a aircraft flight data recorder system uses an electronically erasable solid state memory for storing the flight data and a memory controller circuit are housed in a penetration resistant, thermally insulated enclosure. Power dissipation within the insulated enclosure is minimized by an external switching circuit that applies operating potential to the solid state memory only when data are being transferred to and from the memory circuit. A data protection circuit, located within the insulated enclosure inhibits memory write and erase operations whenever the system operating potential falls below a predetermined level. In continuously storing flight data, the oldest stored data is overwritten with newly arriving flight data and the memory controller maintains an erased boundary that defines the beginning and end of the recorded data. A power monitor circuit, located outside the insulated enclosure, resets the memory controller to the erased boundary following a power interruption. A dedicated portion of the memory space is utilized to store the address of faulty memory locations (detected during the data storage sequence) and stores the beginning and ending memory address of selected portions of the data record. The memory controller is sequenced to skip both the faulty memory locations and memory storage locations associated with the selected portions of the data record when new flight data is being stored.

5. 4,638,452, Jan. 20, 1987, Programmable controller with dynamically altered programmable real time interrupt interval; Ronald E. Schultz, et al., 364/900, 920, 921, 926, 926.9, 927.2, 927.5, 927.8, 927.92, 927.99, 928, 929.2, 931, 931.4, 931.46, 937, 940, 940.1, 941, 941.5, 942, 942.8, 946.2, 948.4, 948.5 , 949, 949.3, 950, 959.1, 964, 965, 965.5, 977 [IMAGE AVAILABLE]

US PAT NO: 4,638,452 [IMAGE AVAILABLE] L10: 5 of 9

ABSTRACT:
A programmable controller includes a main processor which executes a user control program. The main processor is interrupted by a support processor which operates as a real time clock. The interval between interrupts is determined by instructions within the user control program and may be dynamically altered when required. The main processor executes a user created interrupt routine when each interrupt occurs.

6. 4,586,157, Apr. 29, 1986, Memory transfer unit; Robert E. Rector, et al., 364/900; 340/815.04; 364/919, 919.5, 925, 925.2, 925.6, 926.92, 927, 927.2, 927.3, 927.66, 927.92, 927.97, 927.98, 940, 940.2, 941, 941.1, 947, 947.2, 948, 948.2, 948.4, 948.5 , 948.9, 951, 959, 959.1, 964, 964.1, 964.5, 964.6, 965, 965.3, 965.5, 965.76 [IMAGE AVAILABLE]

US PAT NO: 4,586,157 [IMAGE AVAILABLE] L10: 6 of 9

ABSTRACT:
A memory transfer unit is provided which permits replacing messages stored in a message display system with a different set of messages stored in the memory transfer unit. A ci[redacted]t is provided for supplying power from the message display system to [redacted]e memory transfer unit and for inhibiting operation of the memory transfer unit unless the power supply

US PAT NO: 4,484,303 [IMAGE AVAILABLE] L7: 2 of 3

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ABSTRACT:
An improved programmable controller having the ability to use two different data bases while presenting to the outside world a uniform word size. The programmable controller includes pipeline processing and hardware solution of a user control program in a network node format. A memory management scheme is provided allowing for the direct addressability of one-half million words by utilization of a page register. The programmable controller can be incorporated into a network containing other programmable controllers. The programmable controller also incorporates a multi-task interrupt so that the processor can handle more than one job at any particular time. Input/output tasks are handled logically in the scan solving the user networks rather than being based upon a particular physical area of the controller memory.

3. 4,307,447, Dec. 22, 1981, Programmable controller; Salvatore R. Provanzano, et al., 364/200, 221.9, 222, 228.5, 230, 230.3, 231.4, 231.6, 231.8, 232.7, 234, 234.4, 238.3, 242, 242.1, 242.3, 242.94, 243, 243.4, 243.41, 244, 244.3, 244.8, 244.9, 245, 245.1, 254, 254.3, 255.1, 255.2, 255.3, 260.4, 260.7, 261, 262, 262.1, 265, 267, 267.4, 270, 270.3, 280, 280.8 [IMAGE AVAILABLE]

US PAT NO: 4,307,447 [IMAGE AVAILABLE] L7: 3 of 3

ABSTRACT:
An improved programmable controller having the ability to use two different data bases while presenting to the outside world a uniform word size. The programmable controller includes pipeline processing and hardware solution of a user control program in a network node format. A memory management scheme is provided allowing for the direct addressability of one-half million words by utilization of a page register. The programmable controller can be incorporated into a network containing other programmable controllers. The programmable controller also incorporates a multi-task interrupt so that the processor can handle more than one job at any particular time. Input/output tasks are handled logically in the scan solving the user networks rather than being based upon a particular physical area of the controller memory.

=> d l5 1-2 cit,ab
'W3D' IS NOT A RECOGNIZED COMMAND

=> d l5 1-2 cit,ab

1. 4,484,303, Nov. 20, 1984, Programmable controller; Salvatore R. Provanzano, et al., 364/900, 147, 926.9, 927.2, 927.83, 928, 929.2, 933, 933.4, 933.7, 940, 940.1, 940.2, 940.4, 940.61, 940.64, 940.71, 942.3, 942.5, 946.2, 948.3, 948.34, 949, 949.3, 953, 953.4, 962, 964, 964.2, 964.29, 965, 965.4, 965.5, 965.78, 970, 970.5 [IMAGE AVAILABLE]

US PAT NO: 4,484,303 [IMAGE AVAILABLE] L5: 1 of 2

ABSTRACT:
An improved programmable controller having the ability to use two different data bases while presenting to the outside world a uniform word size. The programmable controller includes pipeline processing and hardware solution of a user control program in a network node format. A memory management scheme is provided allowing for the direct addressability of one-half million words by utilization of a page register. The programmable controller can be incorporated into a network containing other programmable controllers. The programmable controller also incorporates a multi-task interrupt so that the processor can handle more than one job at any particular time. Input/output tasks are handled logically in the scan solving the user networks rather than being based upon a particular physical area of the controller memory.

2. 4,307,447, Dec. 22, 1981, Programmable controller; Salvatore R. Provanzano, et al., 364/200, 221.9, 222, 228.5, 230, 230.3, 231.4, 231.6, 231.8, 232.7, 234, 234.4, 238.3, 242, 242, 242.3, 242.94, 243, 243.4, 243.41, 244, 244.3, 244.8, 244.9, 245, 245.1, 254, 254.3, 255.1, 255.2, 255.3, 260.4, 260.7, 261, 262, 262.1, 265, 267, 267.4, 270, 270.3, 280, 280.8 [IMAGE AVAILABLE]



US PAT NO: 4,307,447 [IMAGE AVAILABLE] L5: 2 of 2

ABSTRACT:
An improved programmable controller having the ability to use two different data bases while presenting to the outside world a uniform word size. The programmable controller includes pipeline processing and hardware solution of a user control program in a network node format. A memory management scheme is provided allowing for the direct addressability of one-half million words by utilization of a page register. The programmable controller can be incorporated into a network containing other programmable controllers. The programmable controller also incorporates a multi-task interrupt so that the processor can handle more than one job at any particular time. Input/output tasks are handled logically in the scan solving the user networks rather than being based upon a particular physical area of the controller memory.

=> d l3 cit,ab

1. 4,951,763, Aug. 28, 1990, Checkweigher; Scott E. Zimmerman, et al., 177/164, 185 [IMAGE AVAILABLE]

US PAT NO: 4,951,763 [IMAGE AVAILABLE] L3: 1 of 1

ABSTRACT:
A method and apparatus for in-motion weighing is effectuated by a load cell combined with a means to filter the output thereof and apply the product to a programmable gain amplifier. The programmable gain amplifier's output is filtered and applied to a microprocessor which automatically regulates the programmable gain amplifier according to algorithms which results in an educable system responsive to basic operator initiation commands for determing and setting automatic in-motion weighing functions. Digital filter techniques are use to enhance overall system tolerances.

=> d l2 1-19 cit,ab

1. 5,041,864, Aug. 20, 1991, Image recording apparatus; Takehiko Saito, et al., 355/29, 28, 72 [IMAGE AVAILABLE]

US PAT NO: 5,041,864 [IMAGE AVAILABLE] L2: 1 of 19

ABSTRACT:
An image recording apparatus which is disclosed herein includes a containing section for containing an image recording material which is wound in a rolled form and a body in which the image recording material is utilized for recording an image. The image recording apparatus comprises a feeding device for feeding the image recording material from its one end out of the containing means into the body, a measuring device for measuring the length of the image recording material which is fed out, a cutter for cutting the fed-out portion of the image recording material, a convey mechanism for conveying the cut image recording material pieces within the body to record an image, and a control device for controlling the feeding device and the cutter, so that the image-recording material is fed out and cut up to a length required for removal from the body on the basis of the result of measurement by the measuring device, if the conveying of the image recording material pieces by the convey mechanism is discontinued due to any reason. Therefore, the image recording material pieces of a short length cannot be remained within the body.

operating characteristics are adjusted by an incoming data bit stream from the controlling microprocessor. In addition, in response to data received from a microprocessor, the audio processor is controlled, for example, to have its receive audio path closed and its transmit audio path opened to switch from the receive to transmit mode. Based on digital control data received at predetermined input pins, the audio processor of the present invention has its filter responses, signal paths, and other characteristics altered in a predetermined manner to configure the audio processor to appropriately operate in the transmit and receive modes.

6. 4,944,453, Jul. 31, 1990, Heating system; Artemio Ronzani, 237/8R; 236/46R [IMAGE AVAILABLE]

US PAT NO: 4,944,453 [IMAGE AVAILABLE] L2: 6 of 19

ABSTRACT:
A heating system for buildings, comprising a boiler (12), a liquid circulation pump (28) and an electrical control panel (22), incorporates an electronic economizer device (26) arranged to make the circulation pump (28) operate intermittently according to cycles predetermined by the operator through timers (26a, 26b, 26c).

7. 4,942,556, Jul. 17, 1990, Semiconductor memory device; Toshio Sasaki, et al., 365/200, 49, 207; 371/10.1 [IMAGE AVAILABLE]

US PAT NO: 4,942,556 [IMAGE AVAILABLE] L2: 7 of 19

ABSTRACT:
In a defect relieving technology which replaces defective memory cells of a semiconductor memory device by spare memory cells, use is made of an associative memory. Address information of a defective memory cell is stored as a reference data of the associative memory, and new address information of a spare memory cell is written down as output data of the associative memory. A variety of improvements are made to the associative memory. For instance, a plurality of coincidence detection signal lines of the associative memory are divided into at least two groups, and one group among them is selected by switching means. Reference data of the associative memory comprises three values consisting of binary information of "0" and "1", and don't care value "X". The associative memory further includes a plurality of electrically programable non-volatile semiconductor memory elements.

8. 4,905,305, Feb. 27, 1990, Method and apparatus for controlling the frequency of operation and at least one further variable operating parameter of a radio communications device; Terry N. Garner, et al., 455/183, 186, 315, 317

US PAT NO: 4,905,305 L2: 8 of 19

ABSTRACT:
The operating frequency of a radio transceiver and at least one further variable operating parameter of the radio transceiver are controlled in accordance with pre-stored information. Transmit operating radio frequency information is stored in a memory together with associated optimum modulation deviation level information (e.g., so as to maintain a predetermined modulation level at each operating frequency). Receive operating radio frequency information is similarly stored in the memory along with information indicating whether microprocessor clock oscillator frequency is to be shifted (e.g., so as to avoid spurious interfering harmonics emanating from the clock). When operating in the transmit mode, pre-stored modulation gain level information associated with the selected transmit frequency controls the gain of the modulator circuits to compensate for expected changes in modulator circuit gain with change in transmit radio frequency. In the receive mode, the microprocessor clock oscillator frequency may be shifted in accordance with the selected receive frequency, thereby automatically shifting harmonics of the

microprocessor clock oscillator out of the receiver bandpass when necessary to avoid locally-generated signals from interfering with signal reception.



9. 4,888,618, Dec. 19, 1989, Image forming apparatus having ambient condition detecting means; Tadashi Ishikawa, 355/208, 214, 246, 326 [IMAGE AVAILABLE]w3

ABSTRACT:
An image forming apparatus includes a processor for processing image signals, an image forming system for forming images on recording mediums in accordance with the image signals processed by the processor, the image forming system being capable of forming the images in different colors, a detector for detecting an ambient condition, and a controller for controlling an image forming condition, relating to an image density, of the image forming system in accordance with an output of the detector and a color of image formation by the image forming system.

10. 4,887,311, Dec. 12, 1989, Radio with options board; Terry N. Garner, et al., 455/76, 183, 186, 349

US PAT NO: 4,887,311 L2: 10 of 19

ABSTRACT:
A FM mobile radio is disclosed which is capable of future functional expansion due to a unique microprocessor hardware/software control system. The radio includes a control microprocessor which is capable of performing all the basic radio control functions. In addition, options are added via a plug-on board that includes an option microprocessor which interfaces with the control microprocessor over a data bus and with the radio's audio circuits through audio processing circuitry. The software of the system allows control to be passed to the option board. The radio operates in a standard control mode and an option control mode. In the standard mode, in which no option board is present, the control processor performs all basic radio control functions. In the option mode, where the option control microprocessor is present, the main control processor typically receives commands from the option board.

11. 4,870,699, Sep. 26, 1989, Method and apparatus for controlling the frequency of operation and at least one further variable operating parameter of a radio communications device; Terry N. Garner, et al., 455/76, 62, 67, 115, 125 [IMAGE AVAILABLE]

US PAT NO: 4,870,699 [IMAGE AVAILABLE] L2: 11 of 19

ABSTRACT:
The operating frequency of a radio transceiver and at least one further variable operating parameter of the radio transceiver are controlled in accordance with pre-stored information. Transmit operating radio frequency information is stored in a memory together with associated optimum modulation deviation level information (e.g., so as to maintain a predetermined modulation level at each operating frequency). Receive operating radio frequency information is similarly stored in the memory along with information indicating whether microprocessor clock oscillator frequency is to be shifted (e.g., so as to avoid spurious interfering harmonics emanating from the clock). When operating in the transmit mode, pre-stored modulation gain level information associated with the selected transmit frequency controls the gain of the modulator circuits to compensate for expected changes in modulator circuit gain with change in transmit radio frequency. In the receive mode, the microprocessor clock oscillator frequency may be shifted in accordance with the selected receive frequency, thereby automatically shifting harmonics of the microprocessor clock oscillator out of the receiver bandpass when necessary to avoid locally-generated signals from interfering with signal reception.

vehicle; Mark L. Zeinstra, 381/43; 364/513.5; 381/41, 42 [IMAGE AVAILABLE]



US PAT NO: 4,827,520 [IMAGE AVAILABLE] L2: 12 of 19

ABSTRACT:
A voice actuated control system for controlling vehicle accessories includes a voice processing circuit and memory for storing data representing command words employed to perform control functions for vehicle accessories and for detecting spoken command words and providing data corresponding thereto. A microprocessor compares the data to determine if a word match has occurred and provides a selected control output signal in such event. The microprocessor is coupled by an interface circuit to a plurality of devices to be controlled including data and spoken word to improve the reliability of the system.

13. 4,772,873, Sep. 20, 1988, Digital electronic recorder/player; Virgil D. Duncan, 341/110; 364/724.01; 377/108; 381/31 [IMAGE AVAILABLE]

US PAT NO: 4,772,873 [IMAGE AVAILABLE] L2: 13 of 19

ABSTRACT:
The invention is a digital record/playback apparatus including an input digital filter, and A/D converter, a solid state memory, a D/A converter and an output digital filter. The entire system is driven off a single clock source which allows the frequent response of the filters to be modified simultaneous with the sampling frequency of the A/D and D/A converter. This allows the record/playback apparatus to record low frequency signals, such as medical data, as well as relatively high frequency signals such as voice, by simply changing the frequency of the clock source. In addition, the apparatus includes an expandable memory which allows recording of up to one hour or more of program material.

14. 4,692,601, Sep. 8, 1987, Identification card including switching means for built-in battery; Harumi Nakano, 235/380, 442, 487; 283/75, 904; 902/20 [IMAGE AVAILABLE]

US PAT NO: 4,692,601 [IMAGE AVAILABLE] L2: 14 of 19

ABSTRACT:
An identification card such as an IC card includes a built-in type battery, a central processing unit, a RAM, an FET switch and a latch circuit. An IC card production, the RAM is not energized by the battery when the FET switch is turned off in conjunction with the latch circuit. When the IC card is first used by an card issuer, the RAM is energized by turning on the FET switch in conjunction with the latch circuit.

15. 4,689,553, Aug. 25, 1987, Method and system for monitoring position of a fluid actuator employing microwave resonant cavity principles; Mark L. Haddox, 324/636; 73/149; 324/635; 414/5

US PAT NO: 4,689,553 L2: 15 of 19

ABSTRACT:
A system and method for monitoring position of a piston within a fluid-actuated cylinder by radiating microwave energy into the actuator cylinder and measuring axial position of the piston as a function of microwave resonances and the frequencies at which such resonances occur. sweep a predetermined frequency range for generating one or more TM.sub.01q resonant modes within the cylinder cavity. A threshold detector and a peak detector are coupled to the receiving probe for detecting occurrence of cavity resonances. Latches store oscillator control signals associated with occurrence of up to eight such resonance events, with the stored control signals thus being an indication of resonant frequencies. A microprocessor is programmed to determine cavity

microcomputer.



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'W3D' IS NOT A RECOGNIZED COMMAND

=> d 18 1-29 cit

1. 5,046,029, Sep. 3, 1991, Electronic odo/trip meter for automobiles; Hiroshi Ikeda, 364/561; 235/95R; 377/24.1 [IMAGE AVAILABLE]

2. 5,029,244, Jul. 2, 1991, Control system and methods of making and operating the same; Daniel L. Fowler, 219/497, 492, 501, 505; 307/117 [IMAGE AVAILABLE]

3. 4,994,653, Feb. 19, 1991, Control unit and method of making the same; Brian J. Kadwell, et al., 219/508, 494, 505; 307/117 [IMAGE AVAILABLE]

4. 4,964,075, Oct. 16, 1990, Software and hardware independent auxiliary user programmable intelligent keyboard; Paul J. Shaver, et al., 364/900; 235/146; 341/23; 364/928, 949 [IMAGE AVAILABLE]

5. 4,951,763, Aug. 28, 1990, Checkweigher; Scott E. Zimmerman, et al., 177/164, 185 [IMAGE AVAILABLE]

6. 4,942,556, Jul. 17, 1990, Semiconductor memory device; Toshio Sasaki, et al., 365/200, 49, 207; 371/10.1 [IMAGE AVAILABLE]

7. 4,939,437, Jul. 3, 1990, Motor controller; Samir F. Farag, et al., 318/473, 798, 806; 361/24, 25 [IMAGE AVAILABLE]

8. 4,935,607, Jun. 19, 1990, Control unit and method of making the same; Brian J. Kadwell, et al., 219/508, 494, 497, 505; 364/184; 373/1 [IMAGE AVAILABLE]

9. 4,916,623, Apr. 10, 1990, Electronic postage meter having redundant memory; Frank T. Check, Jr., 364/464.02, 918.52, 944.2, 944.92; 371/68.1 [IMAGE AVAILABLE]

10. 4,911,597, Mar. 27, 1990, Semiconductor processing system with robotic autoloader and load lock; Dan Maydan, et al., 414/217; 118/50, 500, 503, 729; 294/90, 119.1; 414/225, 331, 416, 730, 732, 741, 744.2, 751, 786, 917; 432/239; 901/47

11. 4,908,523, Mar. 13, 1990, Electronic circuit with power drain control; Gregory O. Snowden, et al., 307/43, 18, 66 [IMAGE AVAILABLE]

12. 4,899,034, Feb. 6, 1990, Method of operating a control unit; Brian J. Kadwell, et al., 219/494, 497, 505, 508; 373/7 [IMAGE AVAILABLE]

13. 4,893,248, Jan. 9, 1990, Monitoring and reporting system for remote terminals; W. Hampton Pitts, et al., 364/464.01; 358/84, 86; 364/550; 379/92, 105, 106; 380/10, 20; 455/2, 4, 5 [IMAGE AVAILABLE]

14. 4,881,183, Nov. 14, 1989, Method and apparatus for emission testing; David E. Groe, 364/550, 497, 571.04, 571.08

15. 4,855,772, Aug. 8, 1989, Electronically controlled camera; Isamu Hashimoto, et al., 354/173.1 [IMAGE AVAILABLE]

16. 4,851,652, Jul. 25, 1989, Electronic lock box, access card, system and method; Mir A. Imran, 235/382, 382.5 [IMAGE AVAILABLE]

17. 4,845,632, Jul. 4, 1989, Electonic postage meter system having arrangement for rapid storage of critical postage accounting data in plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 200, 225,

frequencies and the corresponding orders q of each frequency.



16. 4,688,183, Aug. 18, 1987, Fire and security system with multi detector-occupancy-temperature-smoke (MDOTS) sensors; Richard T. Carll, et al., 364/554; 340/506, 514, 825.07; 364/138, 580 [IMAGE AVAILABLE]

US PAT NO: 4,688,183 [IMAGE AVAILABLE] L2: 16 of 19

ABSTRACT:
A fire and security system includes a hierarchical architecture with a central control processor monitoring each of a plurality of multi detector-occupancy-temperature-smoke (MDOTS) sensors mounted in each of the monitored spaces of the building, the MDOTS sensors connected in multi drop fashion in sensor loop networks which are connected to one of a plurality of master controls, each master control monitoring the sensor outputs from one or more sensor loops and reporting the alarm status of any one sensor to the central.

17. 4,535,582, Aug. 20, 1985, Skin packaging machine having microprocessor-based control; Stephen H. Jones, 53/52, 77, 507, 509

US PAT NO: 4,535,582 L2: 17 of 19

ABSTRACT:
A skin packaging machine for the vacuum application of a film over goods to be packaged including a microprocessor-based control. The skin packaging machine includes a film supply, an oven, a film-bearing frame, a base having a platen with a perforated surface, a blower or turbine for drawing a vacuum at the surface, and a variable speed motor for moving the frame from a position adjacent the oven to a position adjacent the perforated surface in order to apply the film to a package on the surface. The microprocessor-based control cooperates with an alphanumeric display to provide a sequential display of machine function parameters which may be individually set, such as the time duration of a particular function. The control arrangement further includes, in a test mode, means for sequentially displaying on the alphanumeric display the condition of sensors and switches.

18. 4,418,571, Dec. 6, 1983, Liquid level measuring system; Einar Asmundsson, et al., 73/304C

US PAT NO: 4,418,571 L2: 18 of 19

ABSTRACT:
A liquid level measuring device has an outer capacitance tube, an imperforate glass tube coaxially within the outer tube defining a capacitor annulus between them, and an inner capacitor sleeve coaxially within the glass tube and having separate longitudinally extending sleeve sections. The separate sleeve sections cooperate with the outer capacitance tube to form a plurality of capacitor sections each having a separately measurable value which varies between dry minimum and submerged maximum.

19. 4,349,882, Sep. 14, 1982, Liquid level measuring system; Einar Asmundsson, et al., 364/509; 73/304C; 377/19, 21

US PAT NO: 4,349,882 L2: 19 of 19

ABSTRACT:
A liquid level measuring system for the underground fuel storage tanks of a fuel dispensing station having a multiple segment capacitance probe in each storage tank and a microcomputer for periodically measuring the capacitance of each segment of each probe and calculating the level and volume of fuel in each tank using capacitance and volume calibration constants automatically updated by the microcomputer from the measured

252.6, 270, 270.1, 273.4, 273.5, 900, 918, 918.52, 925.6, 964, 965, 965.76, 965.79 [IMAGE AVAILABLE]



18. 4,829,161, May 9, 1989, Control unit and method of making the same; Brian J. Kadwell, et al., 219/501, 494, 506, 508; 307/117 [IMAGE AVAILABLE]

19. 4,817,004, Mar. 28, 1989, Electronic postage meter operating system; Paul C. Kroll, et al., 364/464.02, 900, 918, 918.1, 918.52, 939, 939.7, 943.9, 943.91, 944.2, 944.61, 945.4, 945.7, 965, 965.76, 965.79, 976 [IMAGE AVAILABLE]

20. 4,805,109, Feb. 14, 1989, Nonvolatile memory protection arrangement for electronic postage meter system having plural nonvolatile memories; Paul C. Kroll, et al., 364/464.02, 466, 900, 918, 918.1, 918.52, 927.8, 939, 939.7, 941, 941.7, 942.7, 943.9, 943.91, 943.92, 944.61, 948.3, 948.4, 948.5, 964, 965, 965.5, 965.76, 966.1, 966.4, 975.2 [IMAGE AVAILABLE]

21. 4,797,918, Jan. 10, 1989, Subscription control for television programming; Lin N. Lee, et al., 380/20; 358/84, 86; 380/10 [IMAGE AVAILABLE]

22. 4,782,215, Nov. 1, 1988, Control unit and method of making the same; Brian J. Kadwell, et al., 219/494, 497, 505, 508; 364/184; 373/1 [IMAGE AVAILABLE]

23. 4,759,062, Jul. 19, 1988, Arrangement for and method of protecting private security codes from unauthorized disclosure; Gilbert Traub, et al., 380/25; 379/95; 380/23 [IMAGE AVAILABLE]

24. 4,721,947, Jan. 26, 1988, Welding monitor; Kenneth W. Brown, 340/540; 228/56.5, 103; 340/679

25. 4,644,484, Feb. 17, 1987, Stand-alone access control system clock control; Kevin Flynn, et al., 364/569; 328/63; 340/309.15, 825.31; 368/200; 377/16 [IMAGE AVAILABLE]

26. 4,634,846, Jan. 6, 1987, Multimode programmable stand-alone access control system; Roy L. Harvey, et al., 235/382, 375, 435; 340/825.31; D18/41 [IMAGE AVAILABLE]

27. 4,566,106, Jan. 21, 1986, Electronic postage meter having redundant memory; Frank T. Check, Jr., 371/68.1

28. 4,564,922, Jan. 14, 1986, Postage meter with power-failure resistant memory; Arno Muller, 364/900, 917.5, 917.7, 918, 918.5, 918.52, 918.7, 927.2, 928, 935.2, 935.4, 935.45, 935.46, 940, 941, 948.4, 948.5, 949, 959.1, 959.4, 964, 964.1, 965, 965.5, 965.76, 965.78 [IMAGE AVAILABLE]

29. 4,494,114, Jan. 15, 1985, Security arrangement for and method of rendering microprocessor-controlled electronic equipment inoperative after occurrence of disabling event; Norman Kaish, 340/825.31, 426, 571; 364/900, 918, 918.7, 919, 919.2, 920.5, 925, 925.2, 925.6, 927.2, 927.8, 928, 937, 948.4, 948.5, 949, 949.96, 959.1, 964, 965, 965.5, 965.76, 969, 969.3, 969.4 [IMAGE AVAILABLE]

3. 4,924,233, May 8, 1990, Sensor [illegible] with continuous compass interface; Rebecca A. Bird, 342/175, 41; 364/443 [IMAGE AVAILABLE]

US PAT NO: 4,924,233 [IMAGE AVAILABLE] L1: 3 of 7

ABSTRACT:
A sensor input/output system in a main radar system maintains continuous power to the compass interface when the main radar system is shut down. A single level of interrupt handlers is utilized without interrupt nesting or control by task executive software. The sensor input/output system is functionally partitioned such that all of the service required by an interrupt is continuously provided until the service is completed. A digital processor for providing the interrupt servicing and control and PROM firmware for storing the interrupt handlers also have backup power continuously applied. Since the processor compass interrupt handler and compass interface are continuously powered, heading synchronization is maintained by the main radar system during power down conditions.

4. 4,910,776, Mar. 20, 1990, Encryption printed circuit board; John Dyke, 380/25, 4, 21, 23, 29, 44, 49 [IMAGE AVAILABLE]

US PAT NO: 4,910,776 [IMAGE AVAILABLE] L1: 4 of 7

ABSTRACT:
A host computer add on encryption/decryption printed circuit board includes address and control buffers, data buffer and board decode logic having input and output terminals selectively connected to the host computer and to first ports of a dual port random access memory (DPR) for storing a block of data and addresses and inputting portions of the block of data and addresses into the DPR's memory. A central processing unit (CPU) is connected to second ports of the DPR, and to a CPU RAM, CUP ROM, real time clock, key image buffer, and DES encryption device. The CUP pursuant to commands of the host computer fetches: (1) the encryption/decryption key of the key image buffer and information from the DPR for encryption/decryption by the encryption/decryption device; (2) the name from the host computer and date, time and length of access time for accumulating an audit trail stored in the key image buffer; and (3) file, auditor, and supervisor identification keys from key image buffer, and host computer for encryption and after comparison allowing access only to those files associated with these keys. In addition a system station key can be included for encryption and comparison for limiting user access only through an assigned station. A wait generator is connected to the CPU, real time clock and encryption/decryption device for clock synchronization of joint operations.

5. 4,797,918, Jan. 10, 1989, Subscription control for television programming; Lin N. Lee, et al., 380/20; 358/84, 86; 380/10 [IMAGE AVAILABLE]

US PAT NO: 4,797,918 [IMAGE AVAILABLE] L1: 5 of 7

ABSTRACT:
A method and apparatus for one-way subscription television service control which allows the subscribers to subscribe in advance to a variety of programming or to select programming oa a pay-per-view basis.

6. 4,665,397, May 12, 1987, Apparatus and method for a universal electronic locking system; Douglas A. Pinnow, 340/825.56, 825.72; 361/172 [IMAGE AVAILABLE]

US PAT NO: 4,665,397 [IMAGE AVAILABLE] L1: 6 of 7

ABSTRACT:
An apparatus and method for providing a universal electronic locking